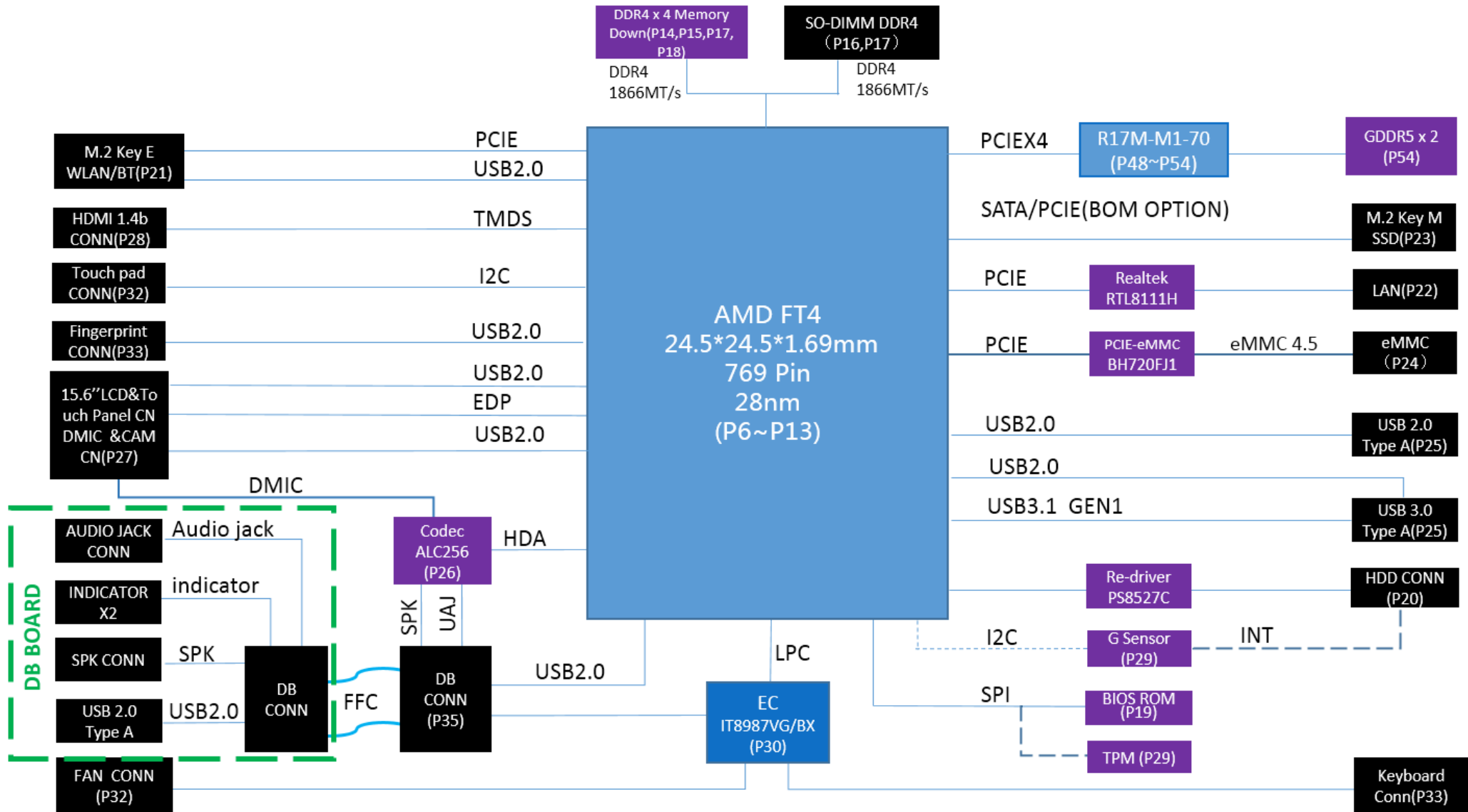


COVER PAGE

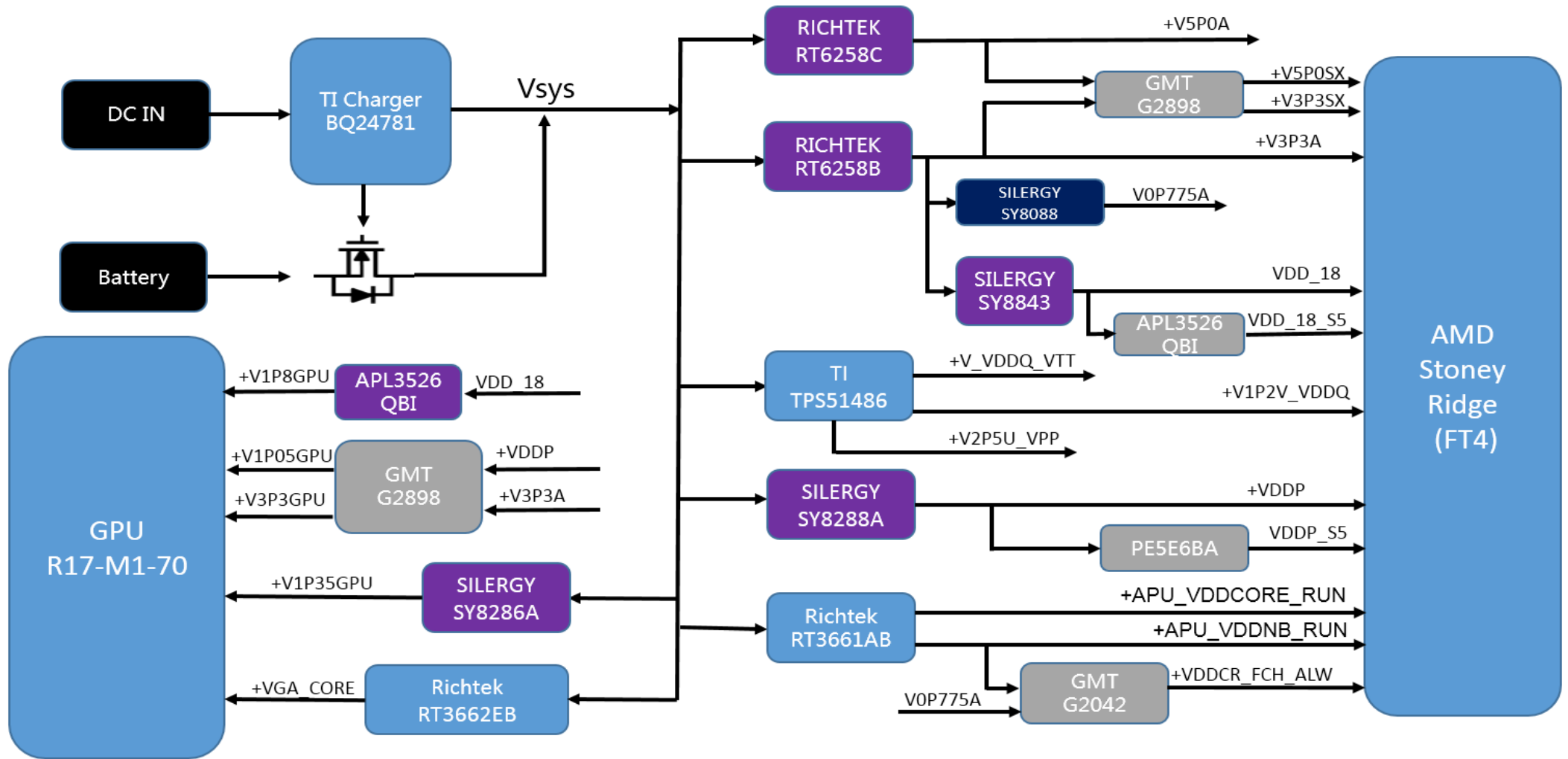
Schematics Page Index (Title / Revision / Change Date)

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04	System List	1.0		38	POWER DELIVERY 5V	1.0	
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06	FT4 MEMORY	1.0		40	POWER DELIVERY 0.95V	1.0	
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10	FT4 CLK/LPC/STAT/SPI/USB	1.0		44	POWER DELIVERY CORE & NB	1.0	
11	FT4 POWER	1.0		45	V1P8GPU/V3P3GPU/V0P95GPU	1.0	
12	FT4 VSS	1.0		46	POWER DELIVERY V1P35GPU	1.0	
13	STRAP	1.0		47	POWER DELIVERY VGA CORE	1.0	
14	MEM MD 0 1	1.0		48	GPU Weston Pro PCIE	1.0	
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16	MEM SODIMM	1.0		50	GPU Weston Pro TMDP	1.0	
17	MEM DECAPS	1.0		51	GPU Weston Pro DP Power	1.0	
18	DDR4 MD TERMINATIONS	1.0		52	GPU Weston Pro Power	1.0	
19	SYSTEM FLASH	1.0		53	GPU Weston Pro MEMORY	1.0	
20	HDD	1.0		54	GPU Weston Pro VRAM x2	1.0	
21	WLAN	1.0		55	Hole & Mark	1.0	
22	LAN	1.0					
23	SSD	1.0					
24	EMMC	1.0					
25	USB	1.0					
26	Audio Codec	1.0					
27	EDP &CAM&MIC	1.0					
28	HDMI CONTROLLER	1.0					
29	TPM&G SENSORS&HALL	1.0					
30	EC(IT8987E)	1.0					
31	RTC	1.0					
32	TouchPad&FAN	1.0					
33	KB CON&KB BLt&FP	1.0					
34	Thermal sensor	1.0					

MB Block Diagram



MB Power Map



Power States(Adapter)

Signal	+VCC3P3_LDO_OUT	+V5P0A	+V3P3A	+V1P8A	+VOP95A	+VOP776A	+VDDCK_PCH_ALW	+V1P2V_VDDQ	+V5P0SX	+V3P3SX	+V1P8SX	+VDDP_S0	+V_VDDQ_VTT	+APU_VDDCORE_RUN	+APU_VDDNB_RUN	+V3P3GPU	+V1P8GPU	+VOP95GPU	+V1P35GPU	+VGA_CORE
S0 (Pull On)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3 (STM)	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S5 (SoftOff)	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Power States(Battery)

Signal	+VCC3P3_LDO_OUT	+V5P0A	+V3P3A	+V1P8A	+VOP95A	+VOP776A	+VDDCK_PCH_ALW	+V1P2V_VDDQ	+V5P0SX	+V3P3SX	+V1P8SX	+VDDP_S0	+V_VDDQ_VTT	+APU_VDDCORE_RUN	+APU_VDDNB_RUN	+V3P3GPU	+V1P8GPU	+VOP95GPU	+V1P35GPU	+VGA_CORE
S0 (Pull On)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3 (STM)	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S5 (SoftOff)	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

BOARD ID

BOARD ID5 1--RUI83 0--RUI91	BOARD ID4 1--RUI82 0--RUI90	BOARD ID3 1--RUI81 0--RUI89	BOARD ID2 1--RUI80 0--RUI88	BOARD ID1 1--RUI79 0--RUI87	BOARD ID0 1--RUI78 0--RUI86
1--DGPU 0--UMA	1--SATA SSD 0--PCI-E SSD	RESERVE	MEMORY ID		

SMBUS/I2C Control Table

	SOURCE	GPU	BATT	IT8987E	SODIMM	Touch Pad	Thermal Sensor	APU	Charger	G-SENSOR Sensor
SM_BAT_CLK SM_BAT_DATA	IT8987E +V3P3A_EC	X	V		X	X	X	X	V	X
SM_THRM_SCL SM_THRM_SDA	IT8987E +V3P3SX_EC	V	X		X	X	V	V APU_SIC APU_SID +V1P8SX	X	X
APU_SMB_CLK APU_SMB_DATA	APU +V3P3SX	X	X	X	V	X	X		X	X
GSEN_I2C0_SCL GSEN_I2C0_SDA	APU +V1P8_GSENSOR	X	X	X	X	X	X		X	V
TOUCHPAD_I2C_CLK TOUCHPAD_I2C_SDA	APU +V3P3A_CP	X	X	X	X	V	X		X	X

PCIe/GFX Port

PCIE	Device
0	LAN
1	WLAN
2	eMMC
3	SSD
GFX	Device
0~3	DGPU

SATA Port

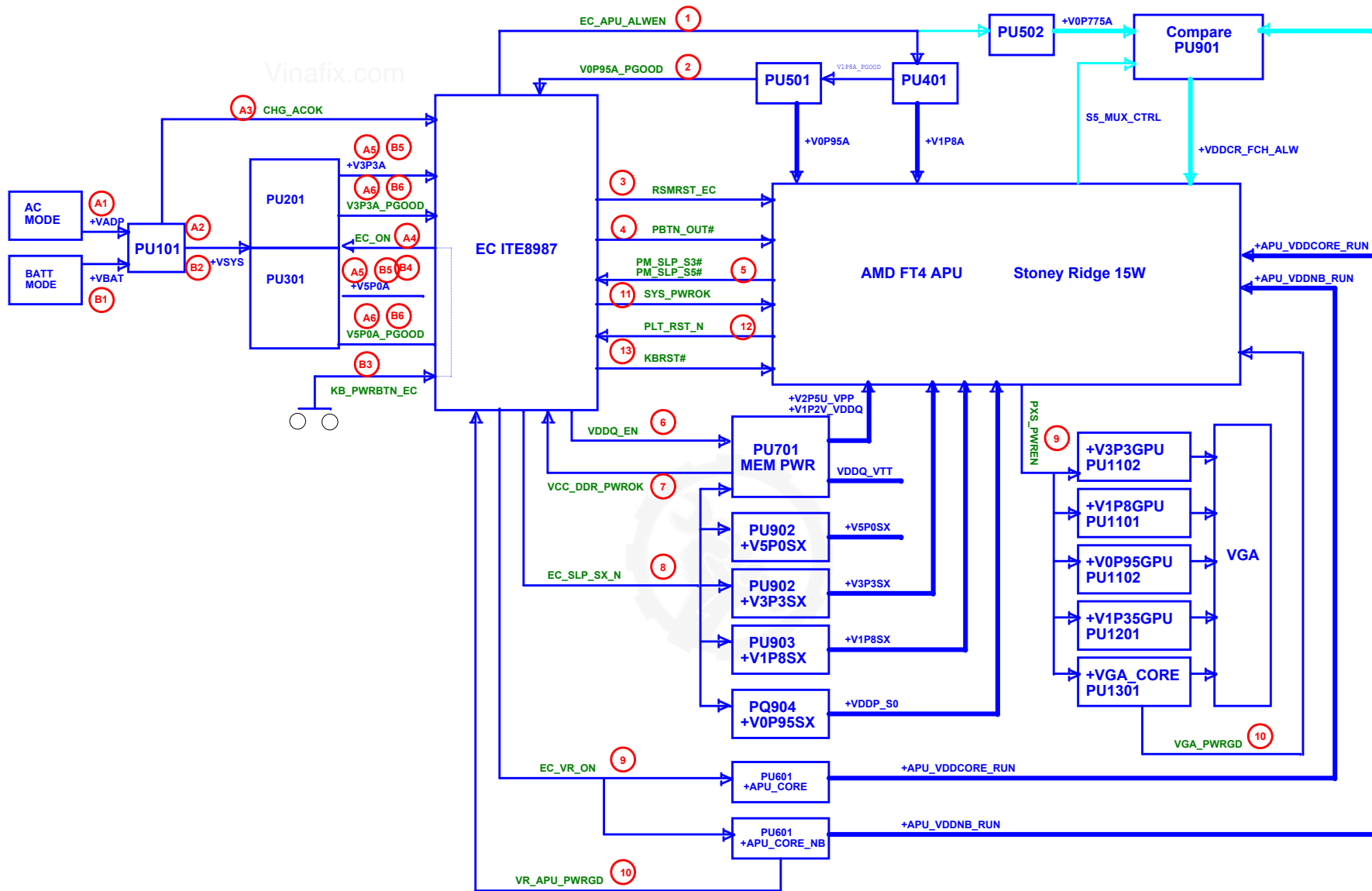
Port	Device
0	HDD
1	SSD

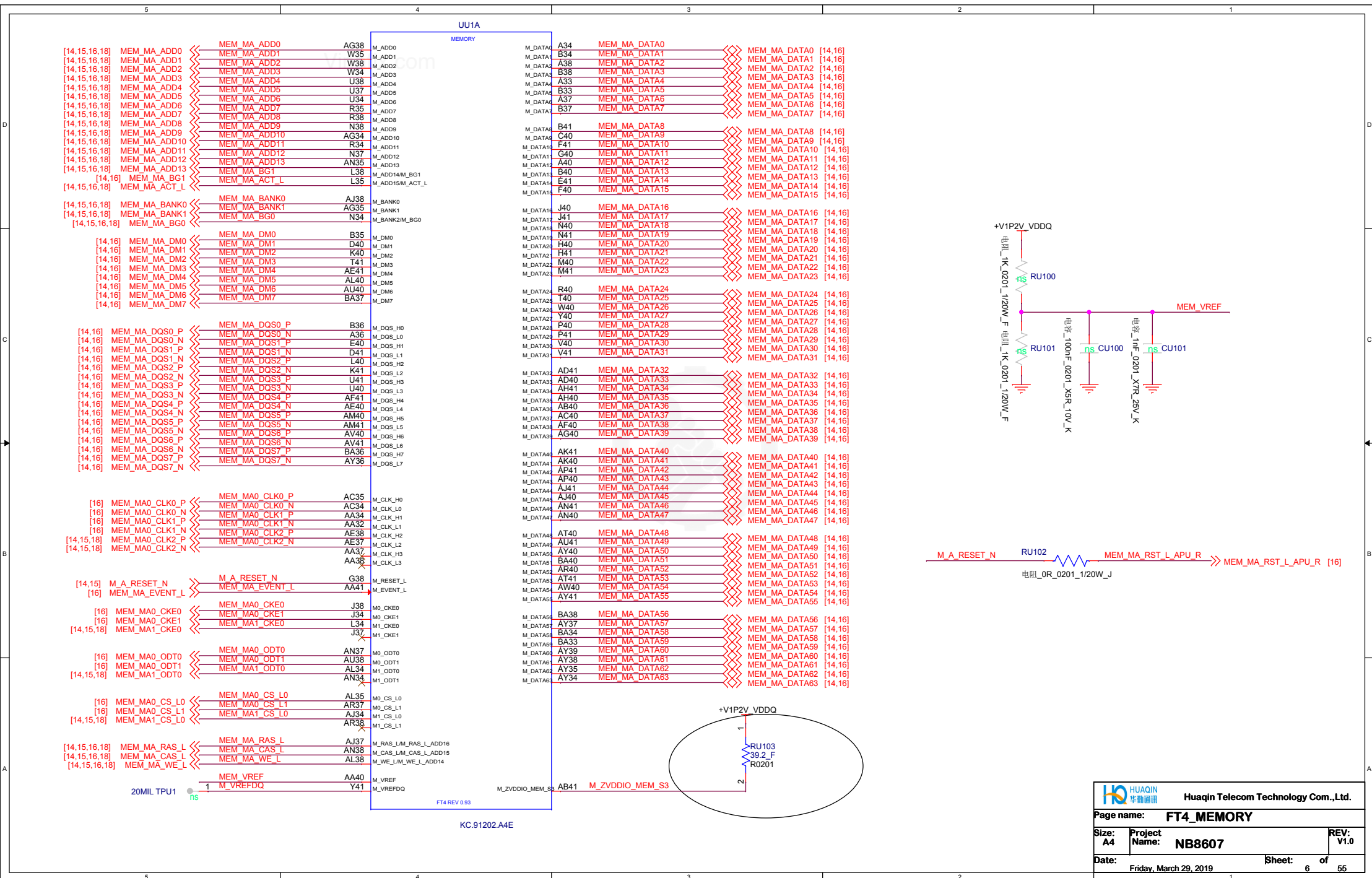
USB2.0 Port

Port	Device
0	Blue Tooth
1	DB USB2.0
2	Finger print
4	USB 3.0 Port
5	USB2.0
6	Touch Panel
7	Camera

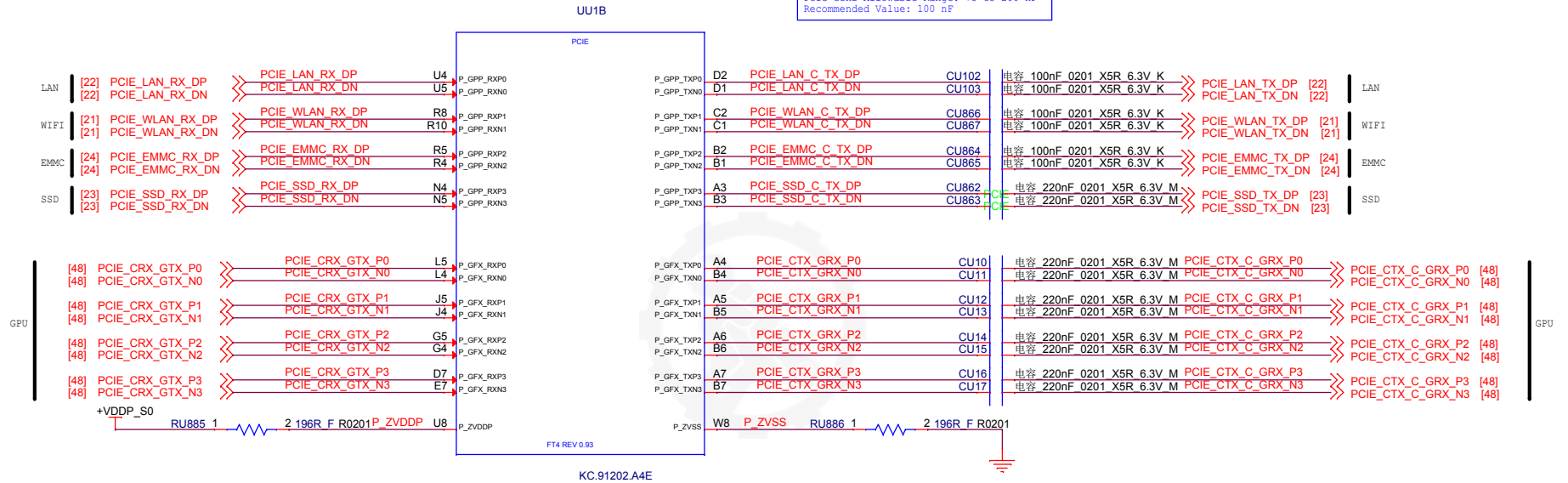
USB3.0 Port

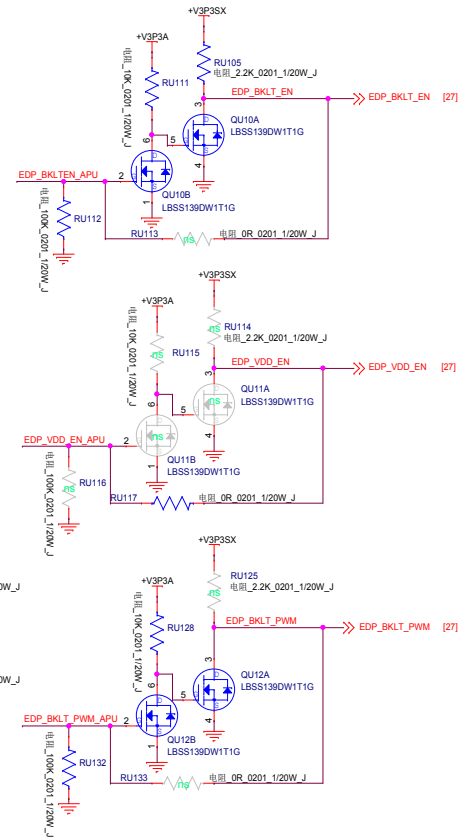
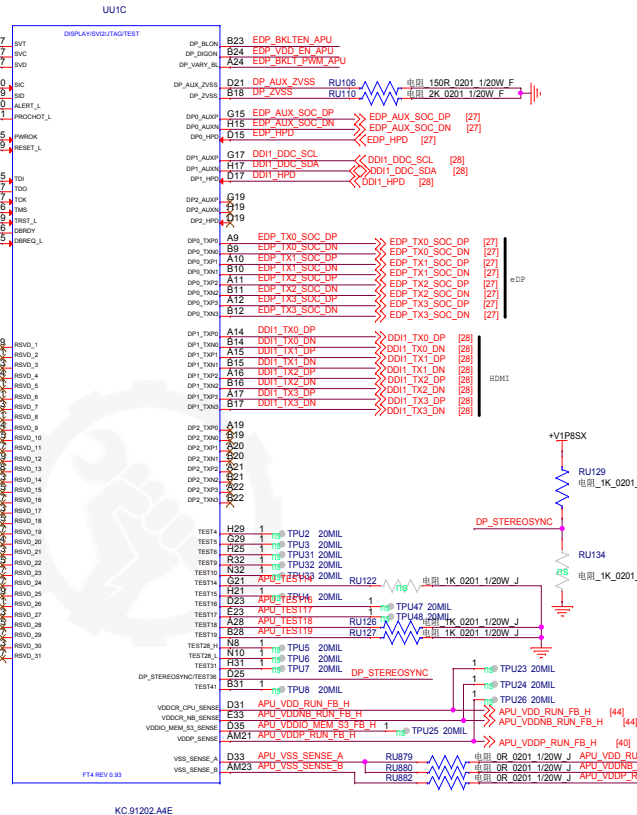
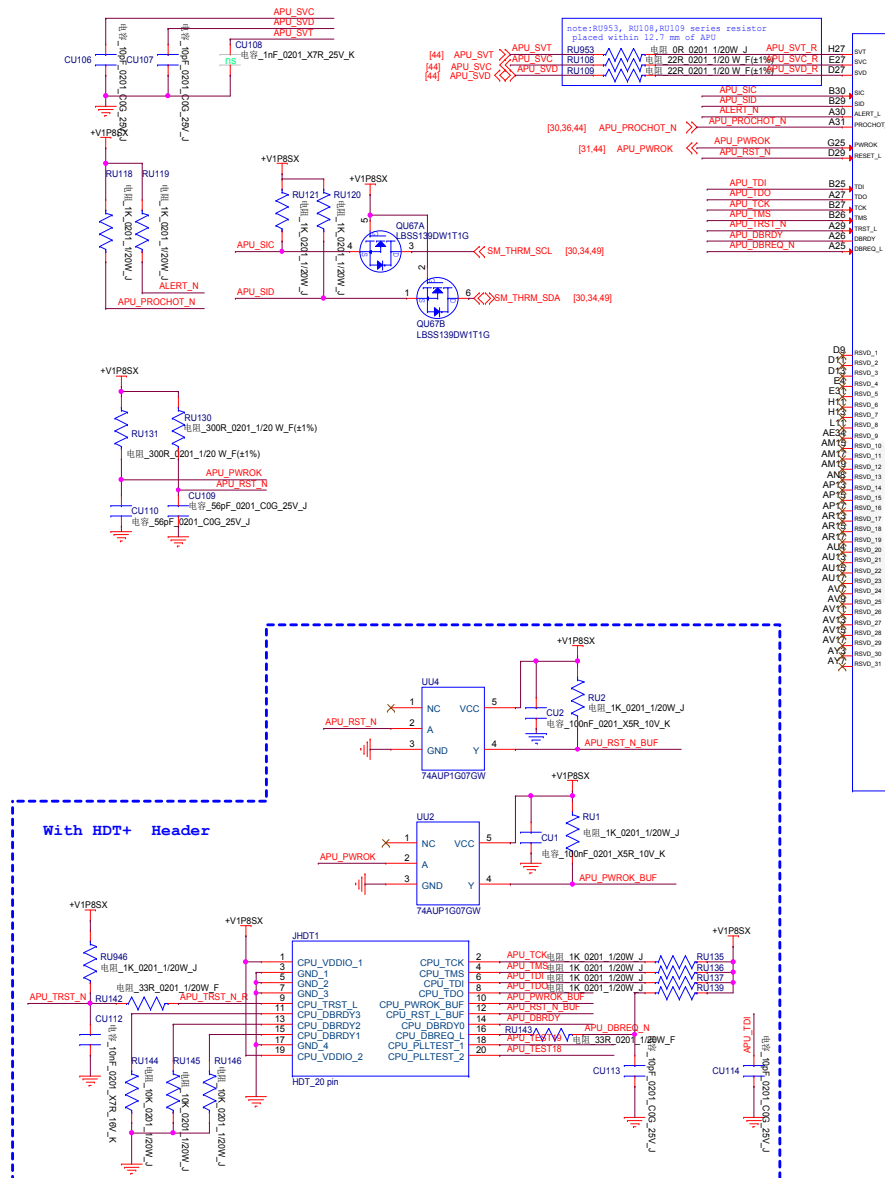
Port	Device
0	USB3.0 Type-A
1	NA

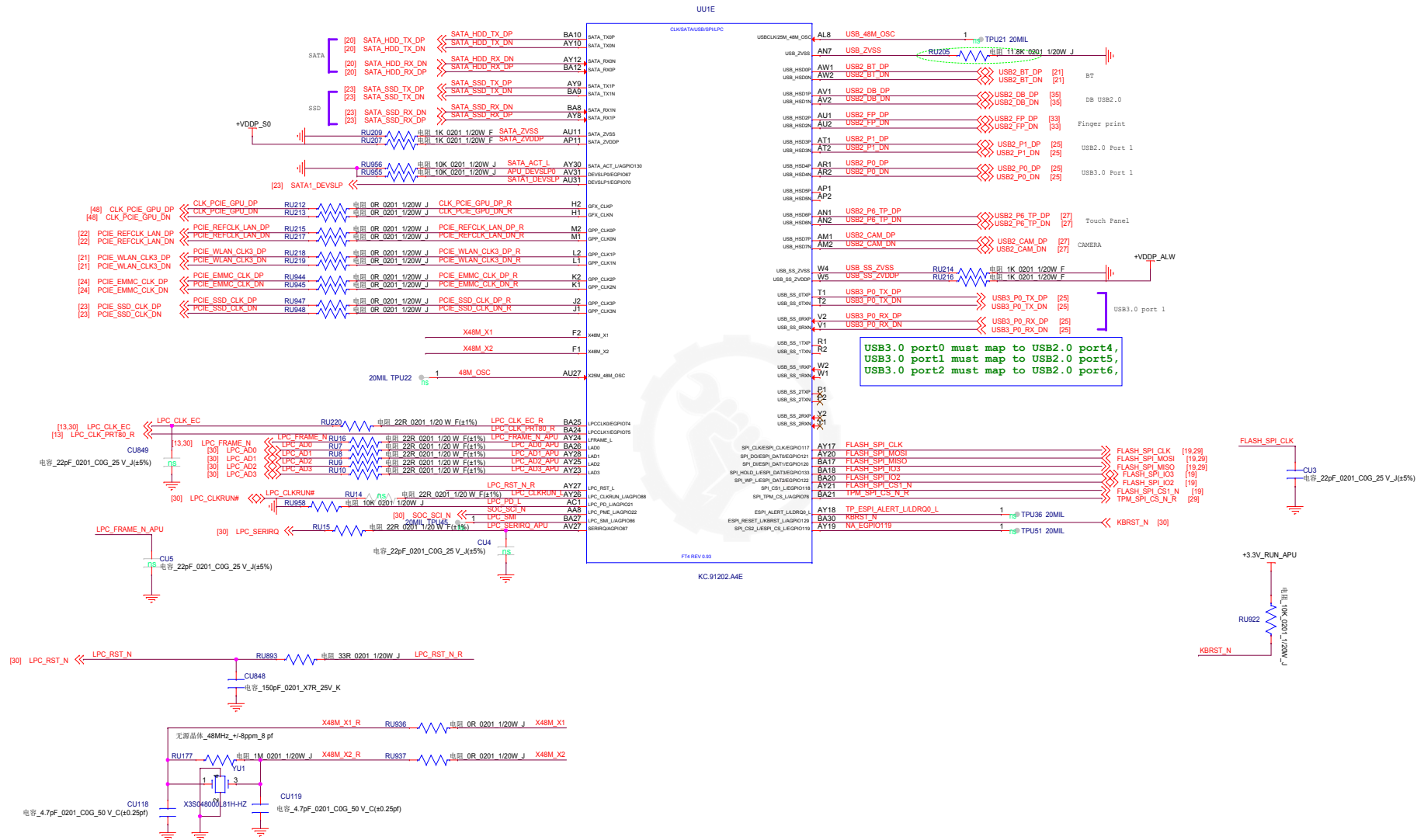




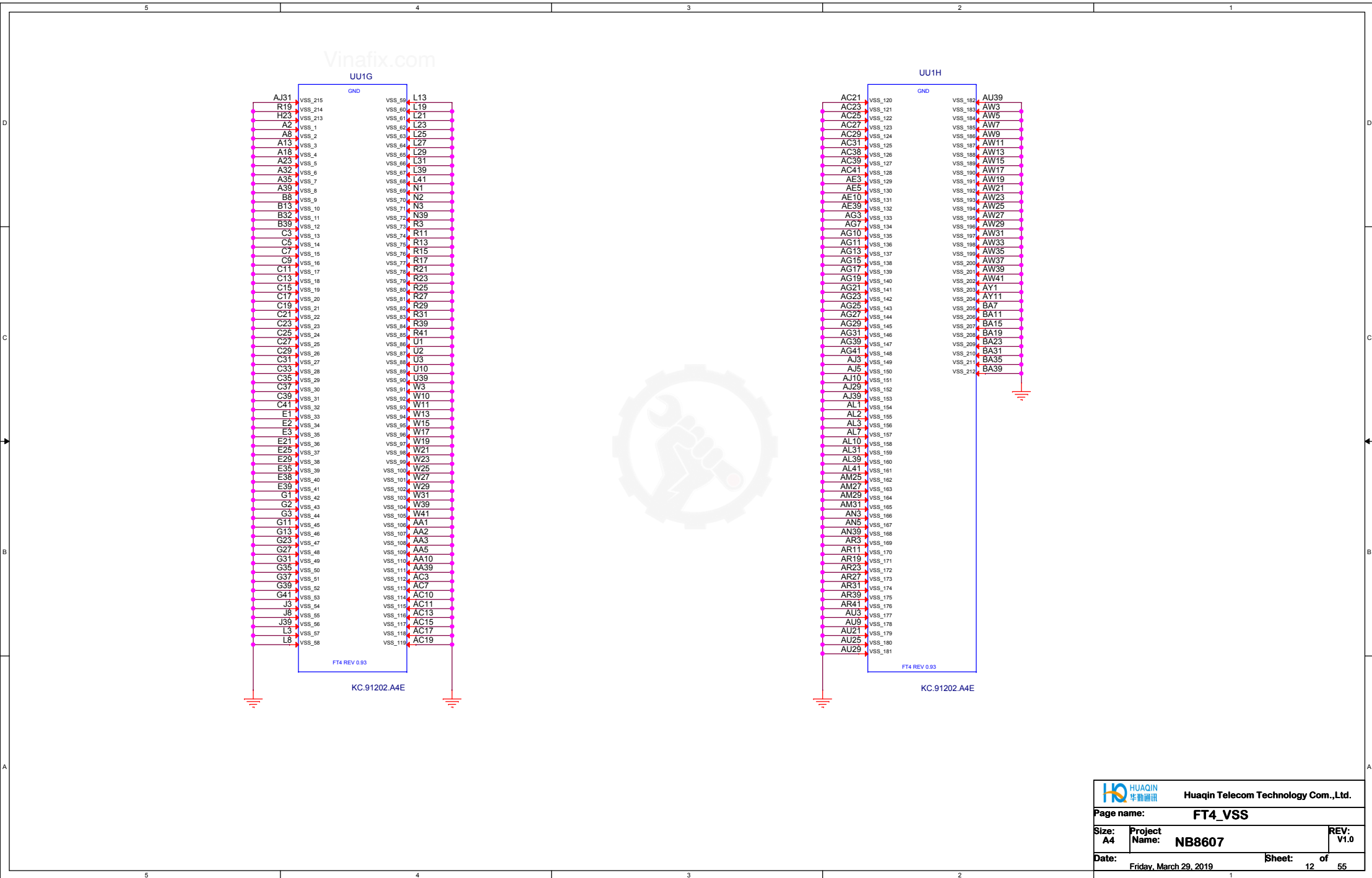
NOTE:
PCIe Gen3 Allowable Range: 176 to 265 nF
Recommended Value: 220 nF
PCIe Gen2 Allowable Range: 75 to 200 nF
Recommended Value: 100 nF

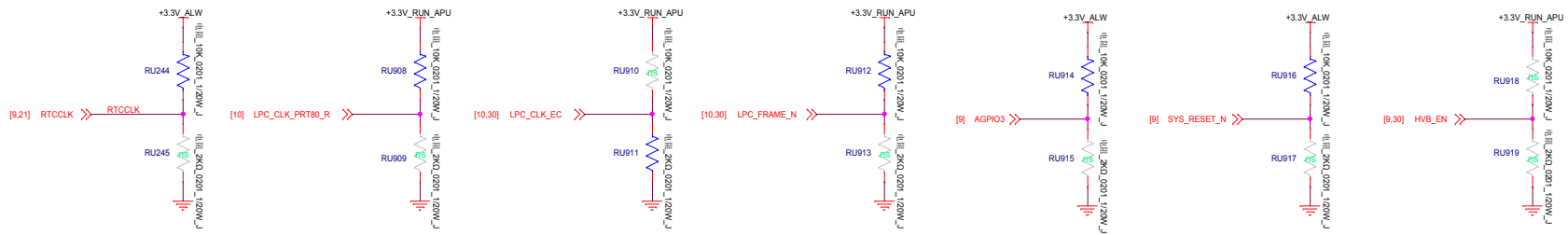




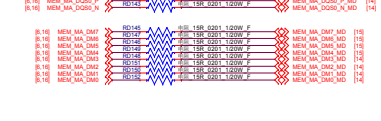
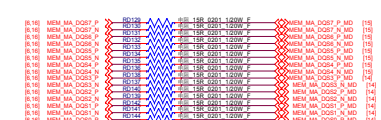
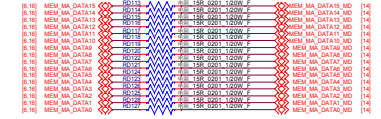
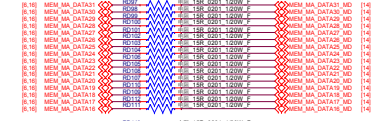
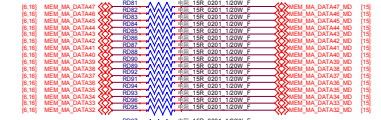
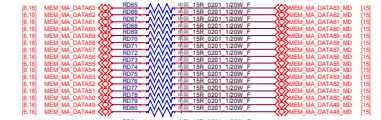
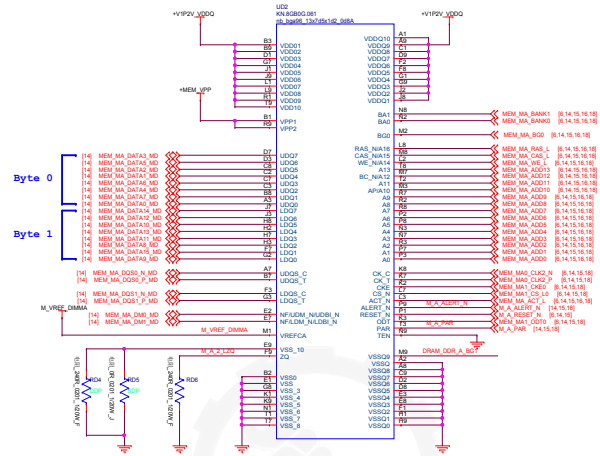
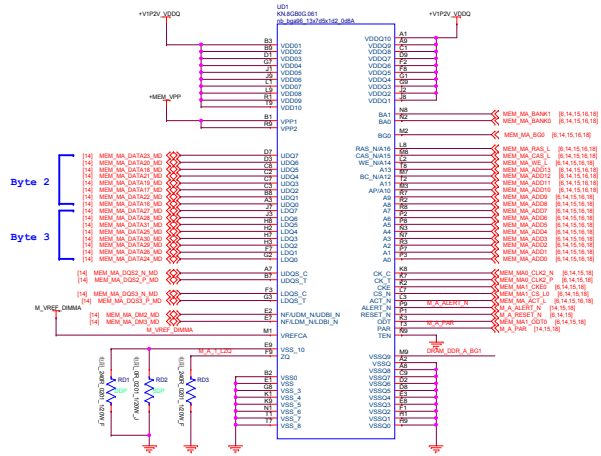


USB3.0 port0 must map to USB2.0 port4,
USB3.0 port1 must map to USB2.0 port5,
USB3.0 port2 must map to USB2.0 port6,

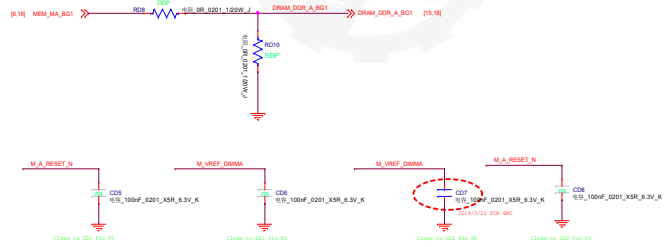
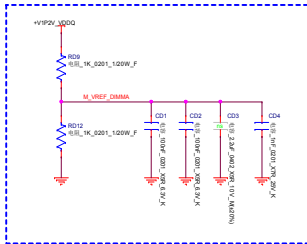




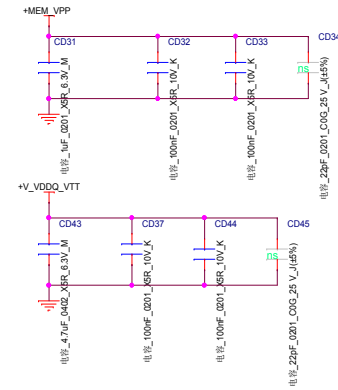
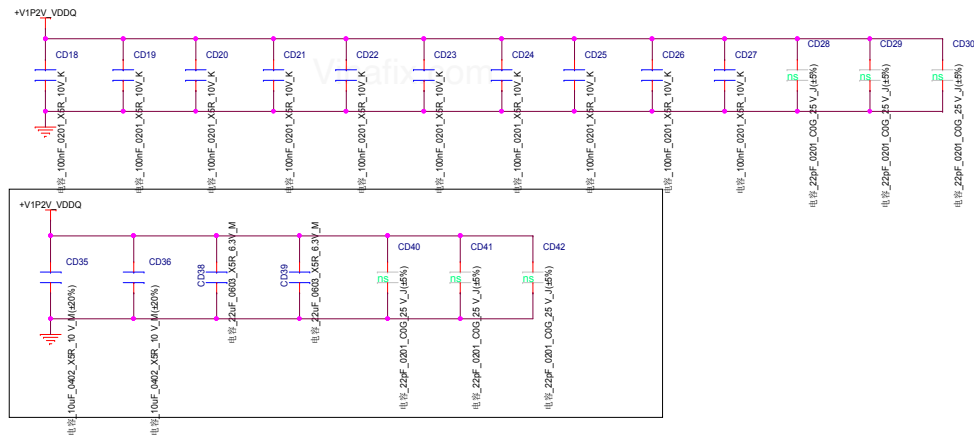
	LPC_CLK0 (LPC_CLK_EC)	LPC_CLK1 (LPC_CLK_PRT80_R)	LFRAME_L	AGPIO3 Int pull-up	RTC_CLK Int pull-up	SYS_RST# Int pull-up	HVB_EN
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	SPI ROM (DEFAULT)	Enhanced reset (for quicker S5 (DEFAULT)	Coin battery is on board. (DEFAULT)	normal reset mode (DEFAULT)	floating Disable HVB
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM	Default to traditional reset logic	Coin battery is not on board.	short reset mode	connected to VSS Enable HVB



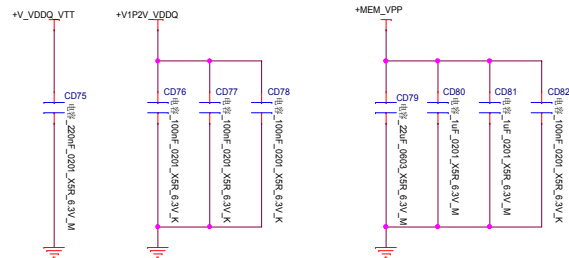
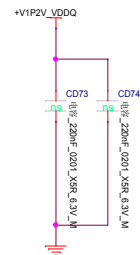
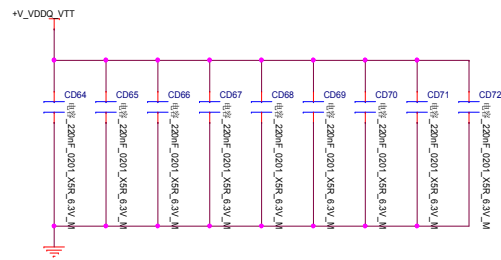
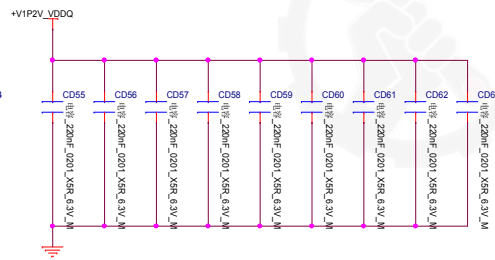
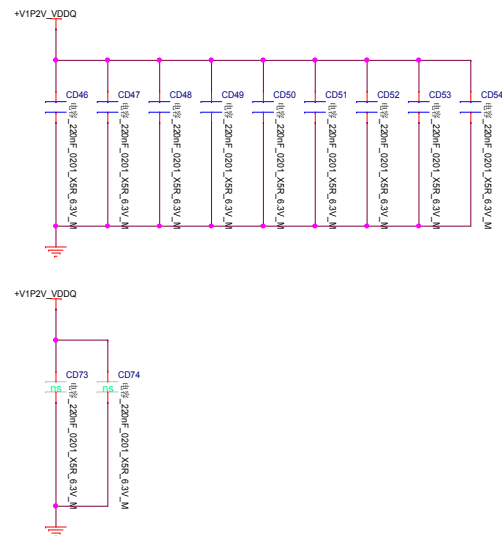
SDRAM REF GENERATION



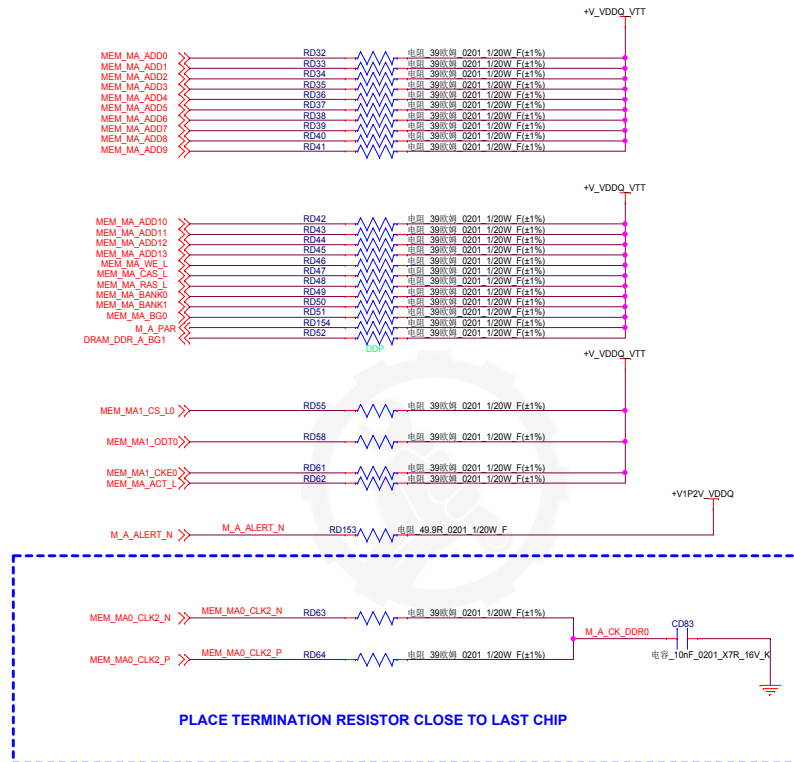
Layout Note: Place near SODIMM



DECOUPLING CAPACITORS FOR MEMORY DOWN

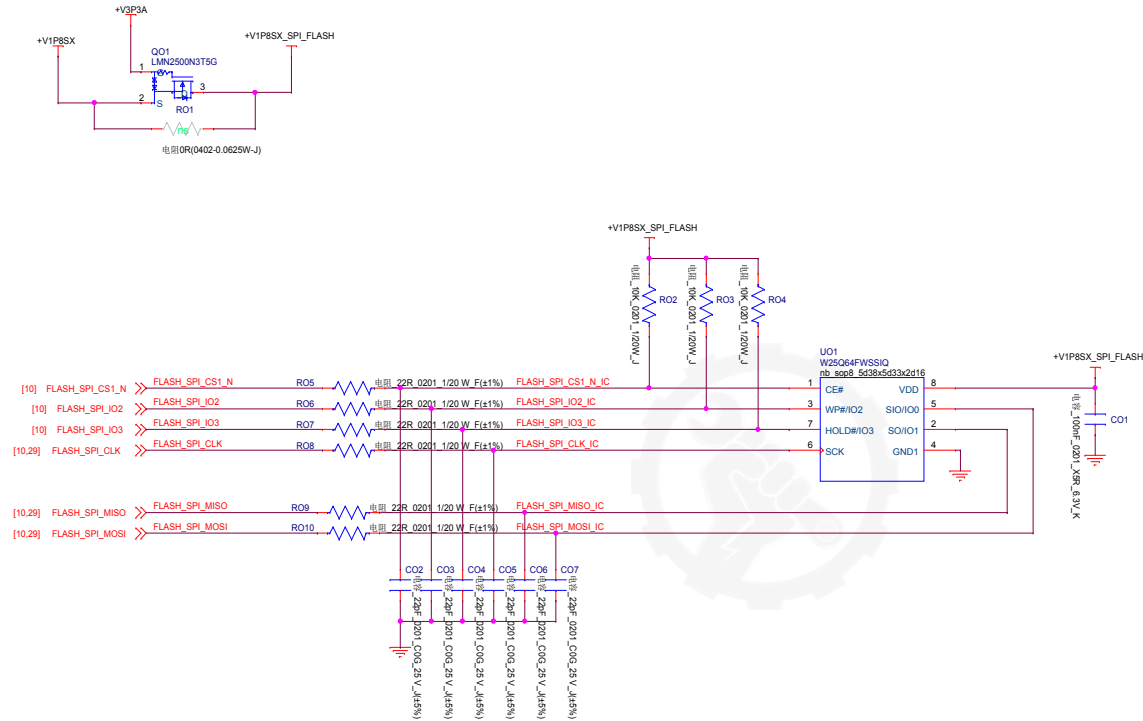
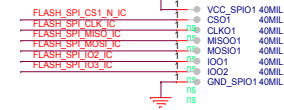


MEMORY TERMINATIONS FOR MEMORY DOWN

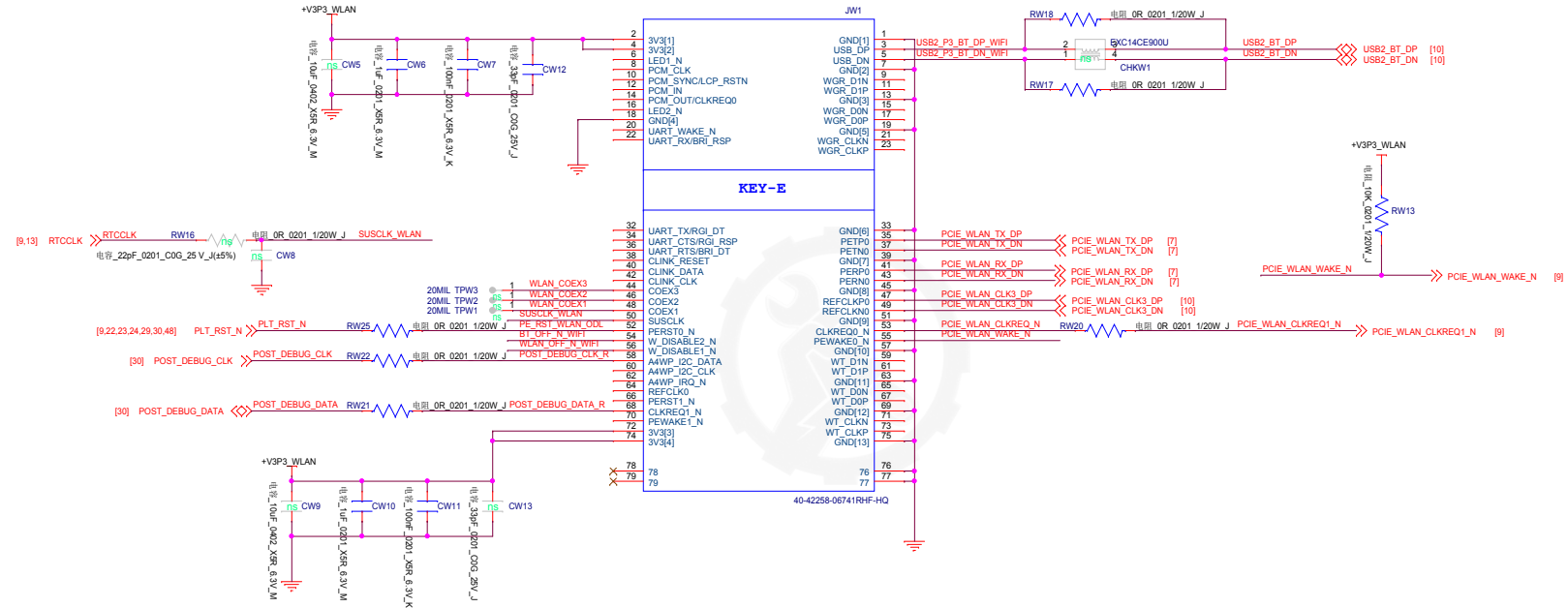
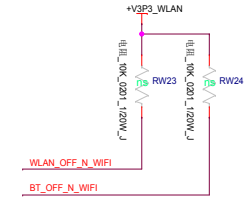
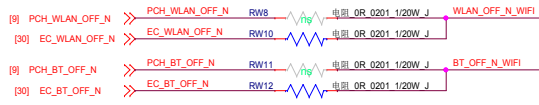
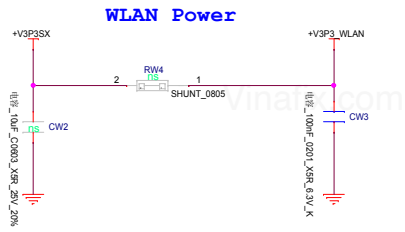


FOR product line

+V1P8SX_SPI_FLASH

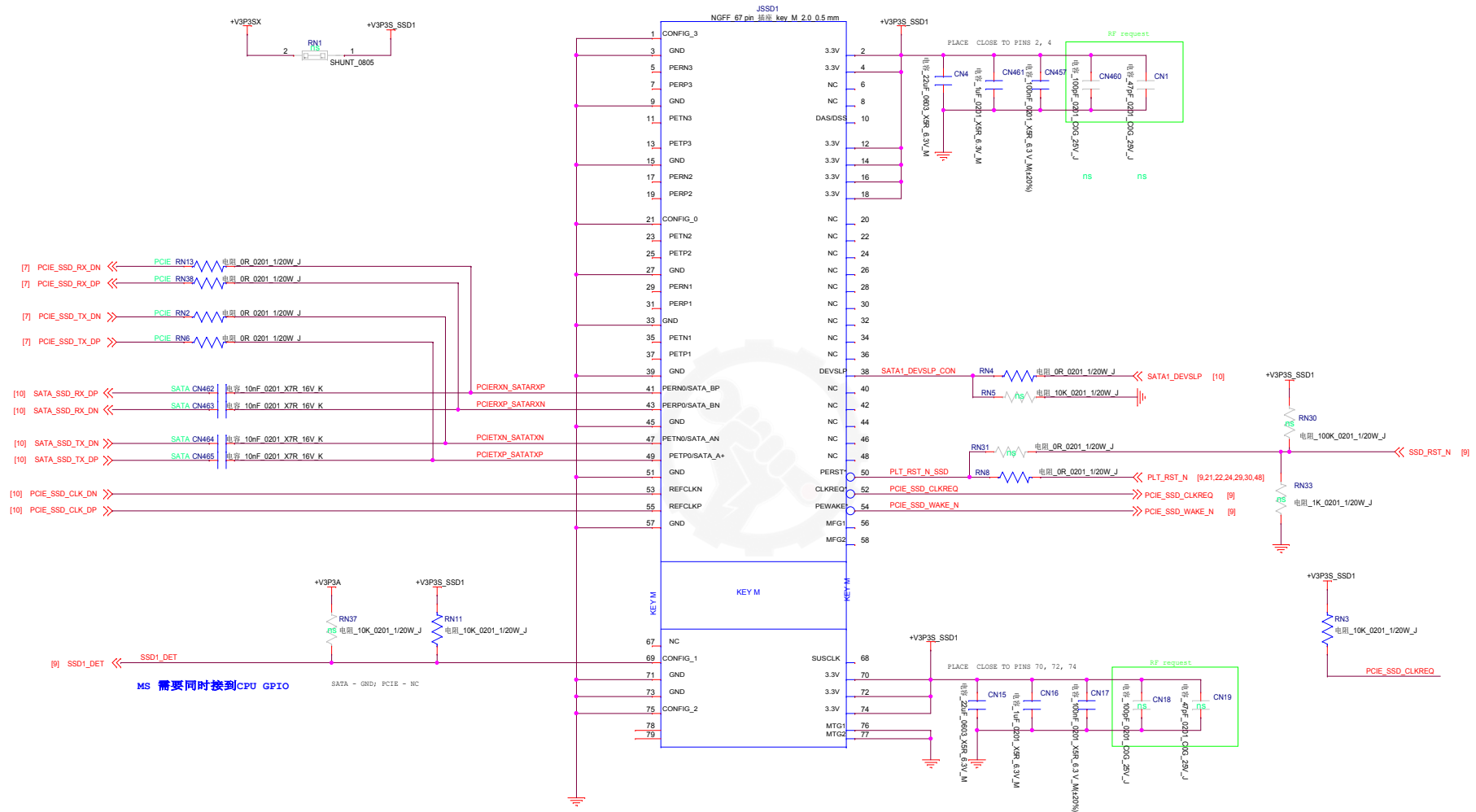


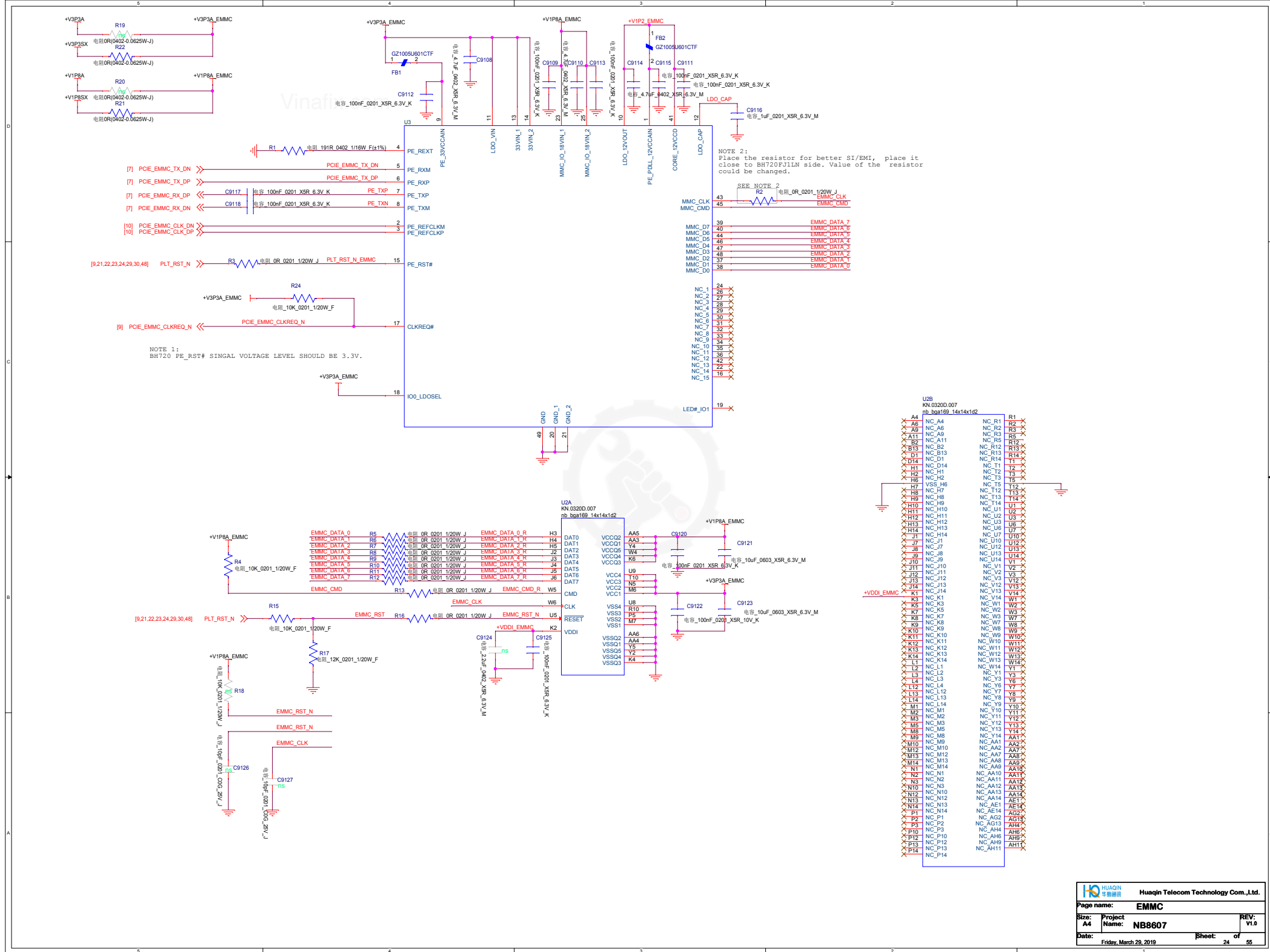
WLAN



SSD CONN

Vinafix.com

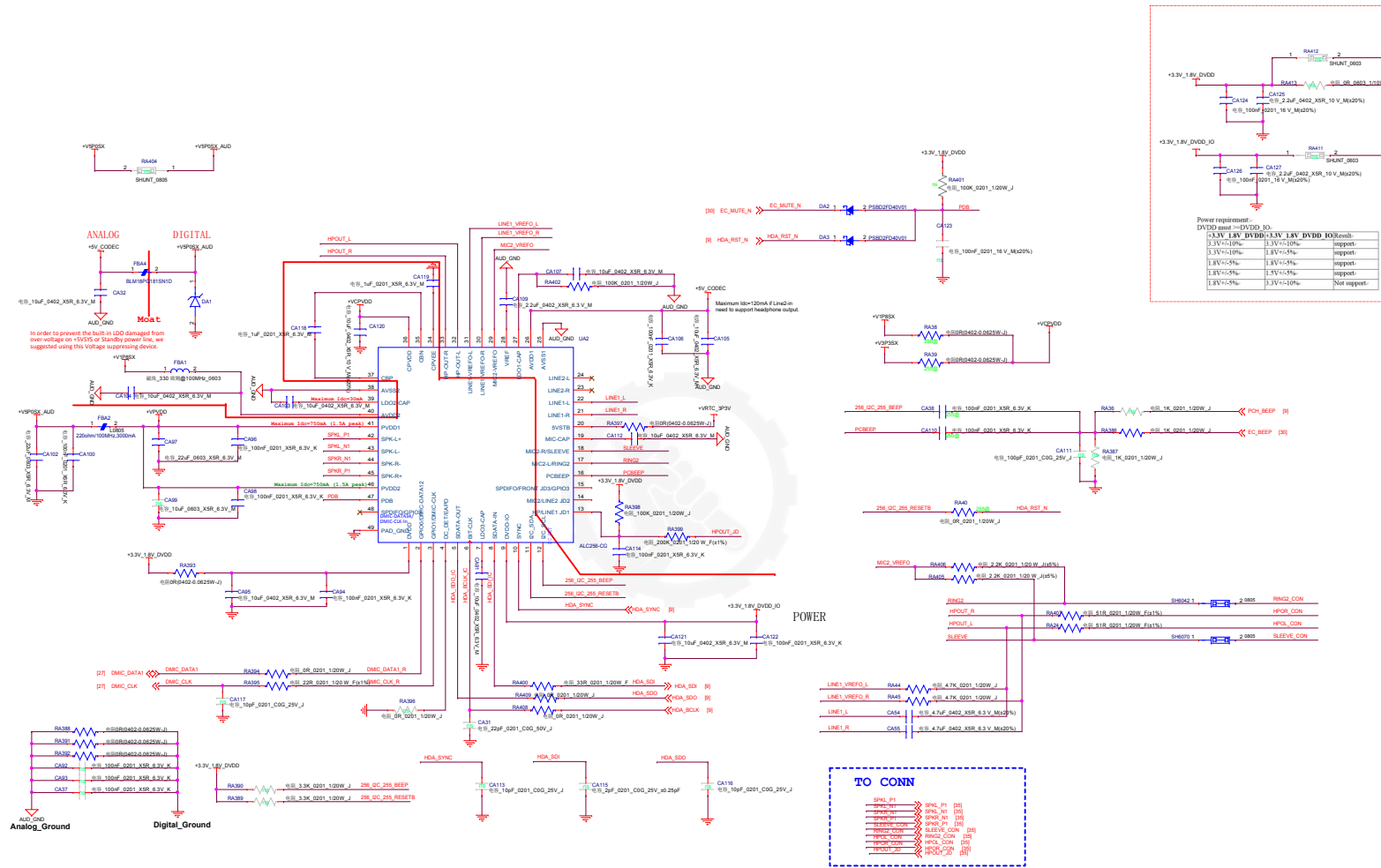




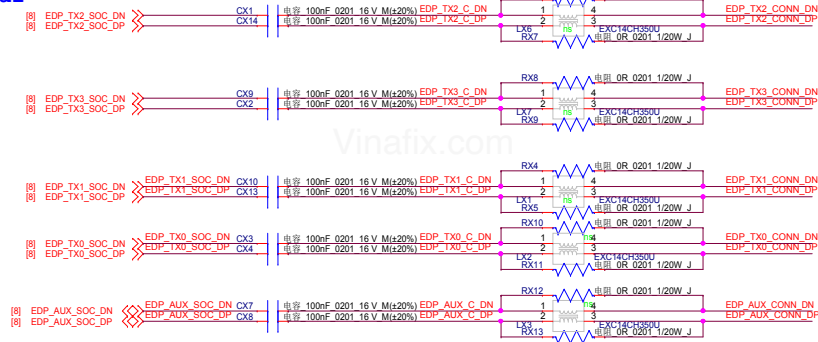
NOTE 2:
Place the resistor for better SI/EMI, place it
close to BH720F3J1LN side. Value of the resistor
could be changed.

NOTE 1:
BH720 PE_RST# SINGAL VOLTAGE LEVEL SHOULD BE 3.3V.

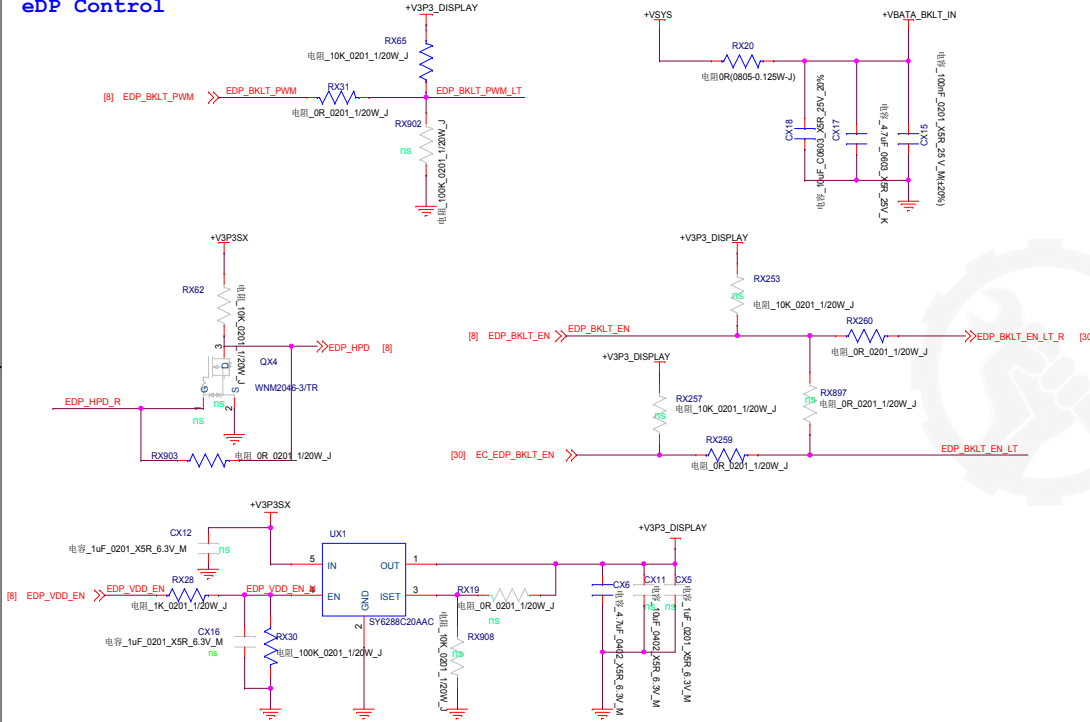
U2B	KN 0320D.007	nb_bga169 14x14x1d2
A4	NC_A4	NC_R1
A5	NC_A6	NC_R2
A6	NC_A8	NC_R3
A7	NC_A9	NC_R5
B2	NC_A11	NC_R12
B13	NC_B2	NC_R12
D1	NC_B13	NC_R14
D14	NC_D1	NC_T1
H1	NC_D14	NC_T1
H2	NC_H1	NC_T2
H3	NC_H2	NC_T3
H7	VSS_H6	NC_T5
H8	NC_H7	NC_T12
H9	NC_H8	NC_T13
H10	NC_H9	NC_T14
H11	NC_H10	NC_U1
H12	NC_H11	NC_U2
H13	NC_H12	NC_U3
H14	NC_H13	NC_U6
J1	NC_H14	NC_U7
J7	NC_J1	NC_U10
J8	NC_J2	NC_U11
J9	NC_J8	NC_U13
J10	NC_J9	NC_U14
J11	NC_J10	NC_V2
J12	NC_J11	NC_V3
J13	NC_J12	NC_V3
J14	NC_J13	NC_V12
K1	NC_J14	NC_V13
K3	NC_K1	NC_V14
K5	NC_K3	NC_W1
K7	NC_K5	NC_W2
K8	NC_K7	NC_W3
K9	NC_K8	NC_W7
K10	NC_K9	NC_W8
K11	NC_K10	NC_W9
K12	NC_K11	NC_W10
K13	NC_K12	NC_W11
K14	NC_K13	NC_W12
L2	NC_K14	NC_W13
L3	NC_L2	NC_W14
L4	NC_L3	NC_Y3
L12	NC_L4	NC_Y8
L13	NC_L12	NC_Y7
L14	NC_L13	NC_Y8
M1	NC_L14	NC_Y9
M2	NC_M1	NC_Y10
M3	NC_M2	NC_Y11
M5	NC_M3	NC_Y12
M6	NC_M5	NC_Y13
M8	NC_M6	NC_Y14
M9	NC_M8	NC_Y14
M10	NC_M9	NC_AA1
M12	NC_M10	NC_AA2
M13	NC_M12	NC_AA7
M14	NC_M13	NC_AA8
N1	NC_M14	NC_AA9
N2	NC_N1	NC_AA10
N3	NC_N2	NC_AA11
N10	NC_N3	NC_AA12
N12	NC_N10	NC_AA13
N13	NC_N12	NC_AA14
N14	NC_N13	NC_AE1
P1	NC_N14	NC_AE14
P2	NC_P1	NC_AG2
P3	NC_P2	NC_AG13
P10	NC_P3	NC_AH4
P12	NC_P10	NC_AH6
P13	NC_P12	NC_AH9
P14	NC_P13	NC_AH11
NC_P14		



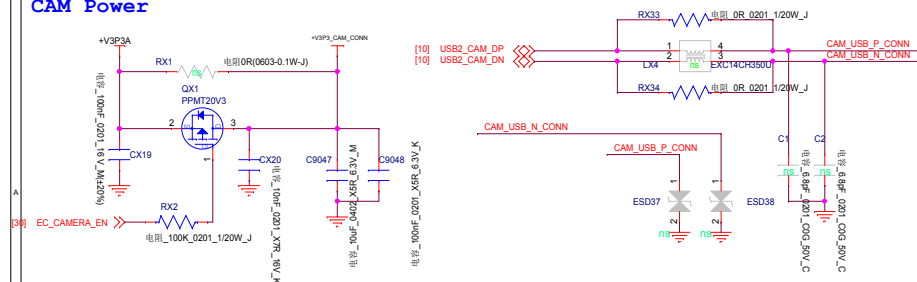
eDP Signal



eDP Control

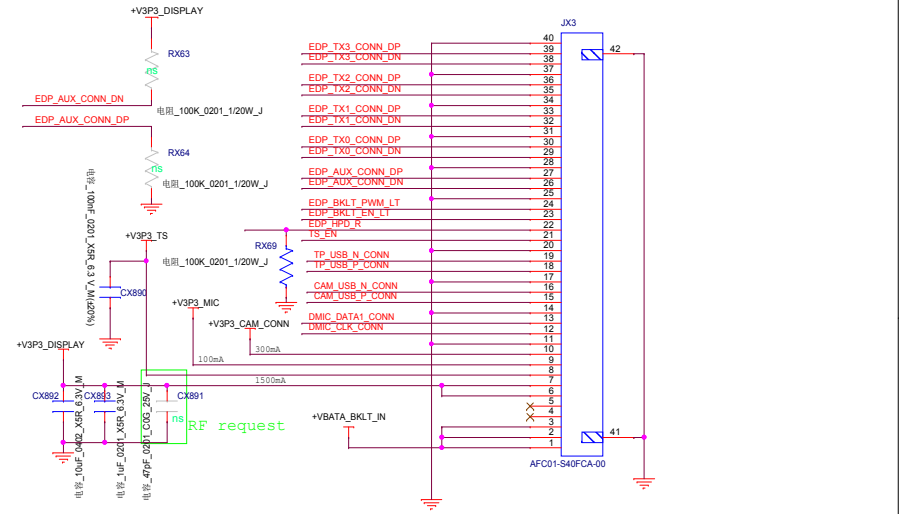


CAM Power

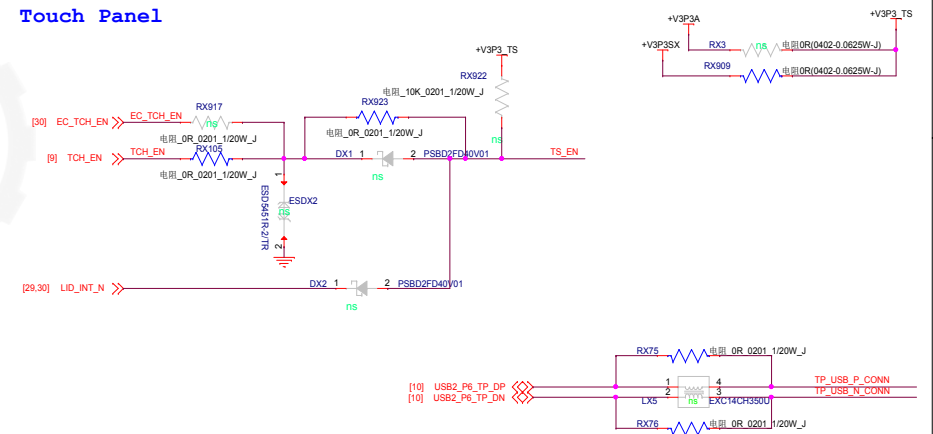


MIC

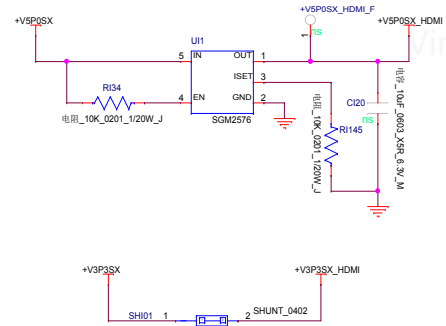
eDP & CAM & DMIC & Touch Panel CONN



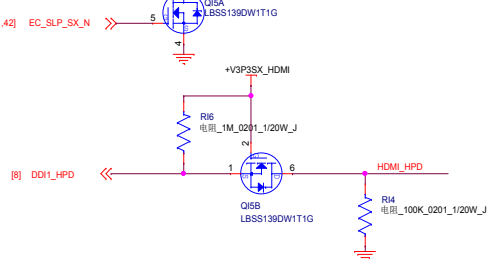
Touch Panel



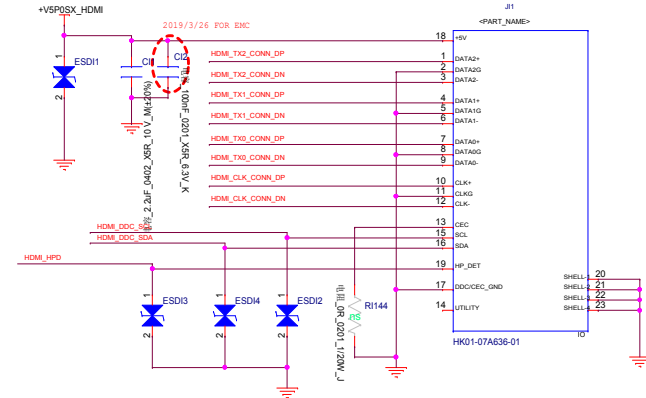
HDMI power



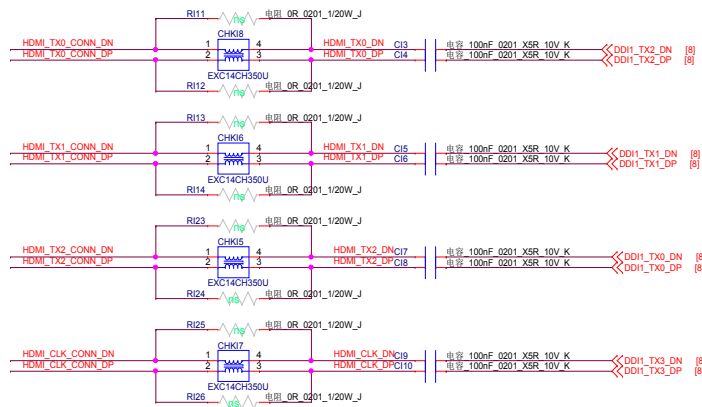
[30.41.42] EC_SLP_SX_N



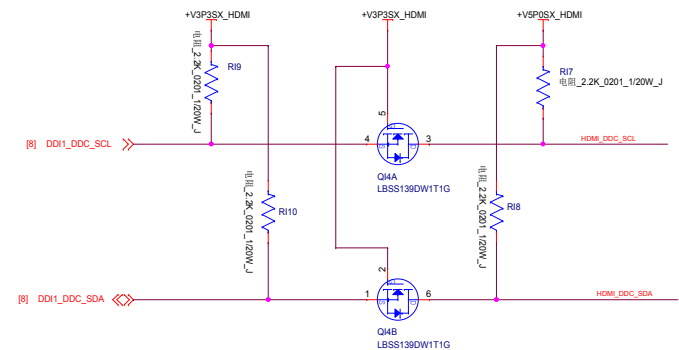
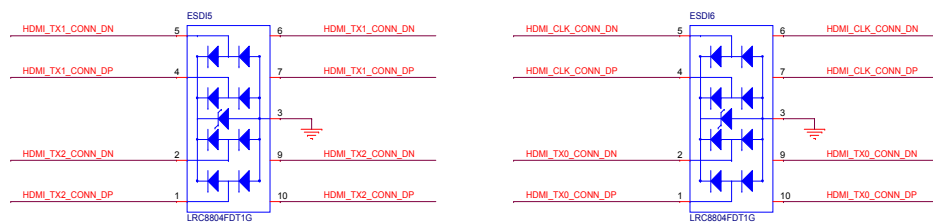
HDMI CONN



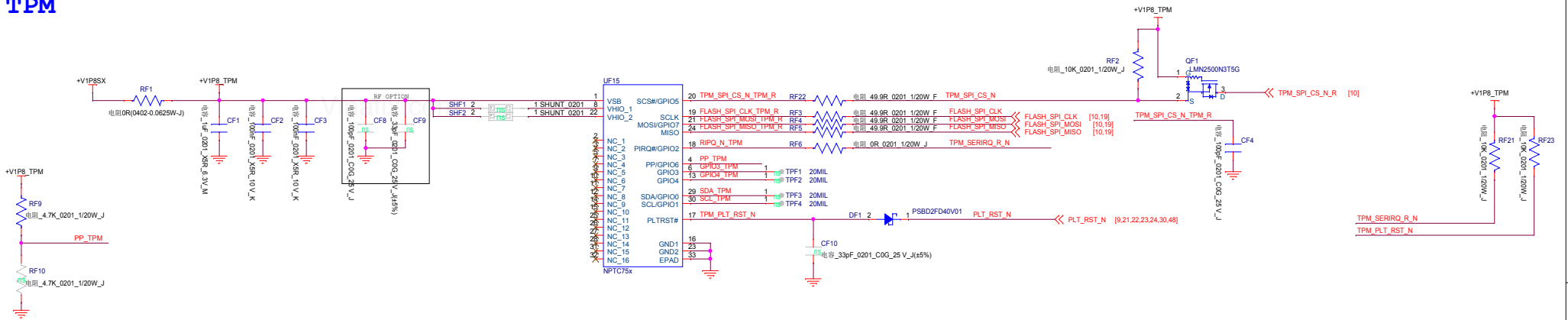
Signal



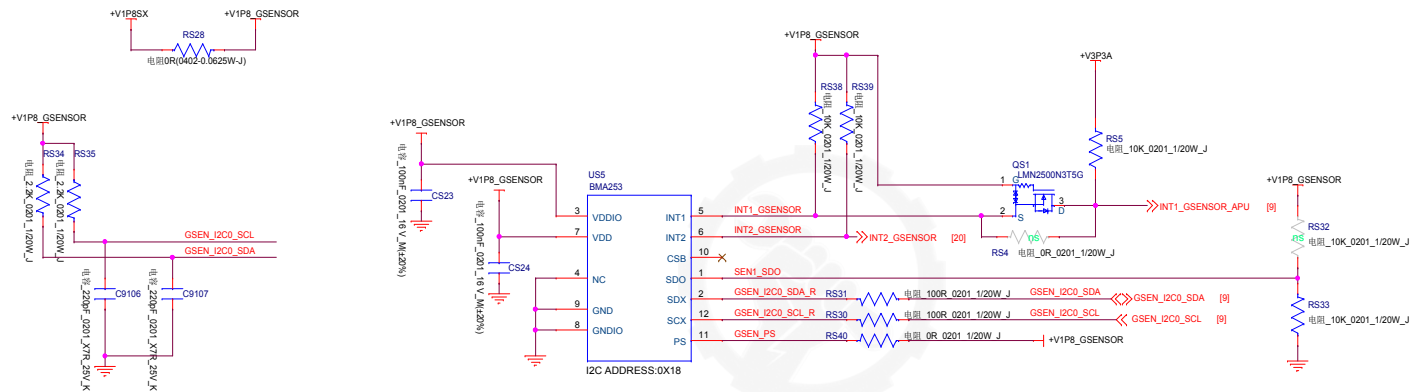
ESD



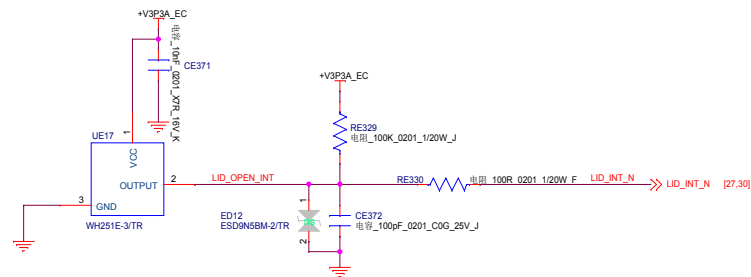
TPM

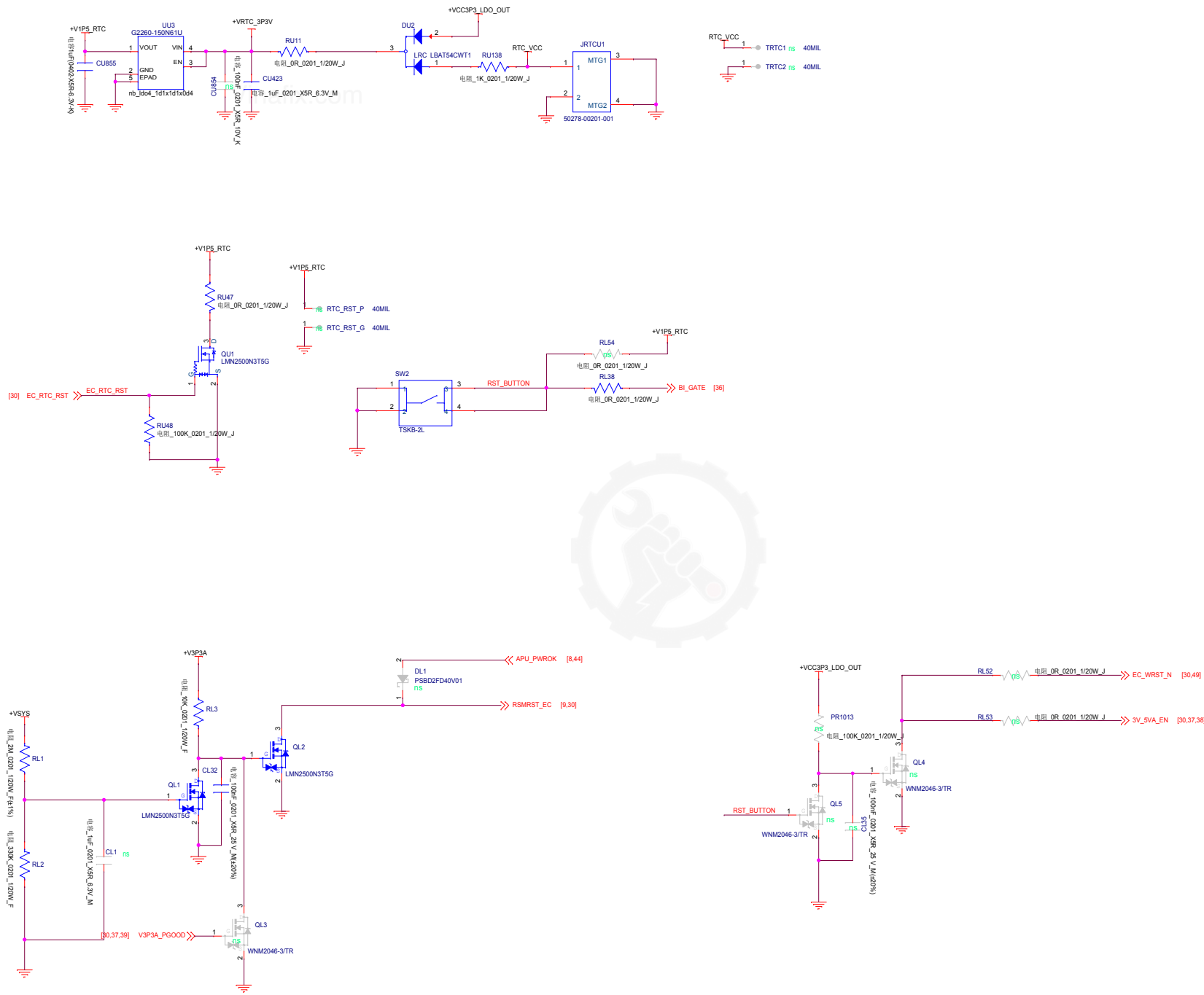


G-SENSOR

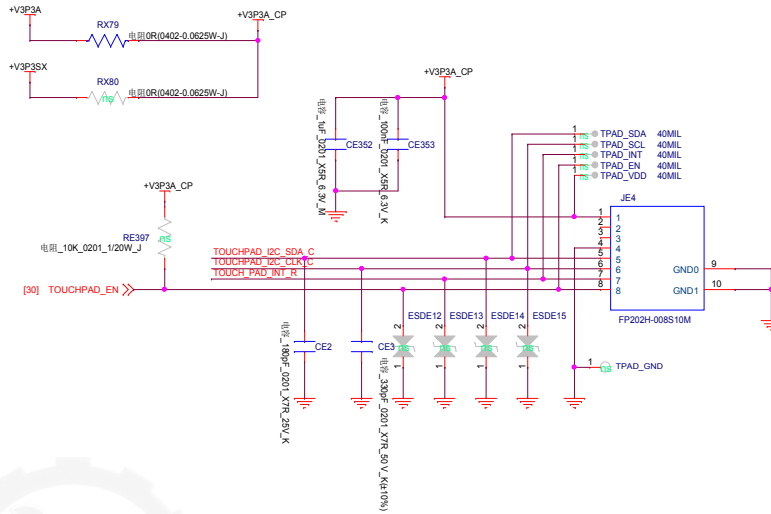
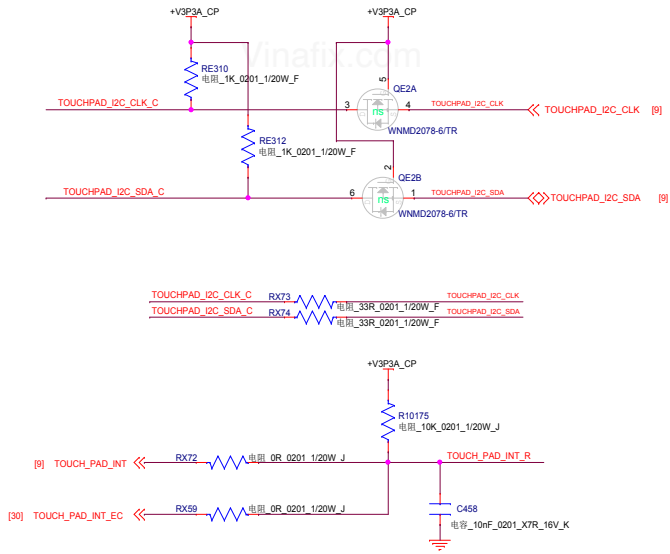


Hall-SENSOR

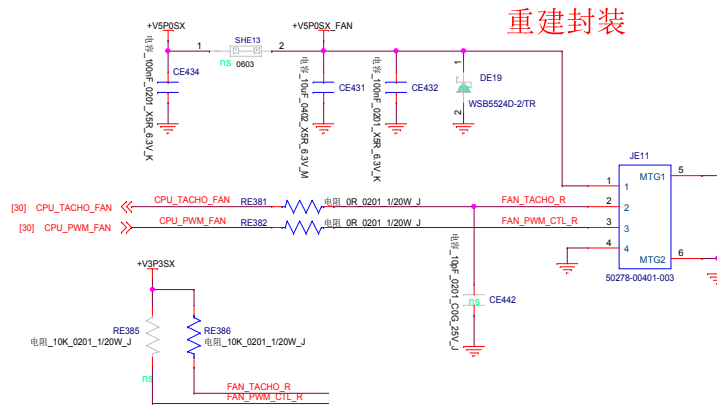




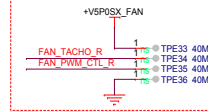
TOUCH PAD



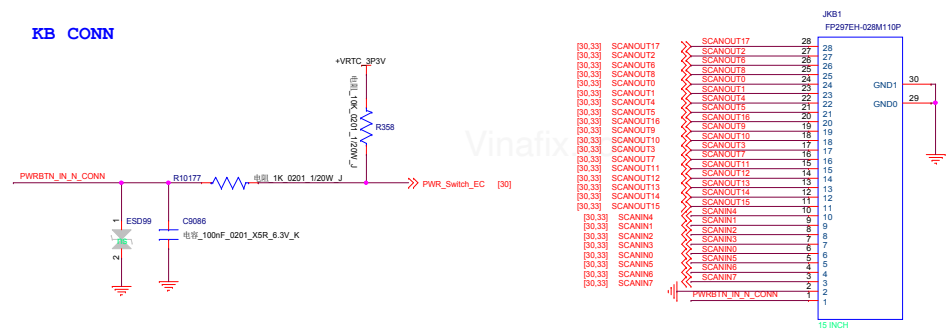
FAN CONN



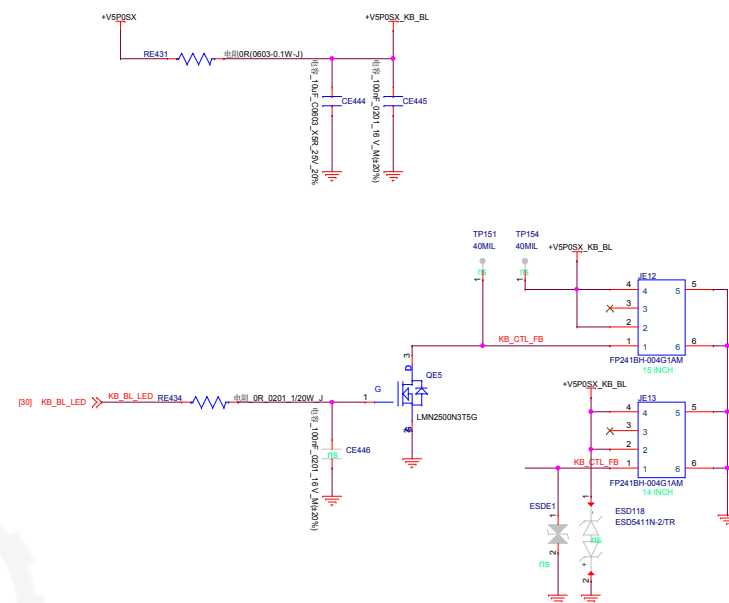
重建封装



KB CONN



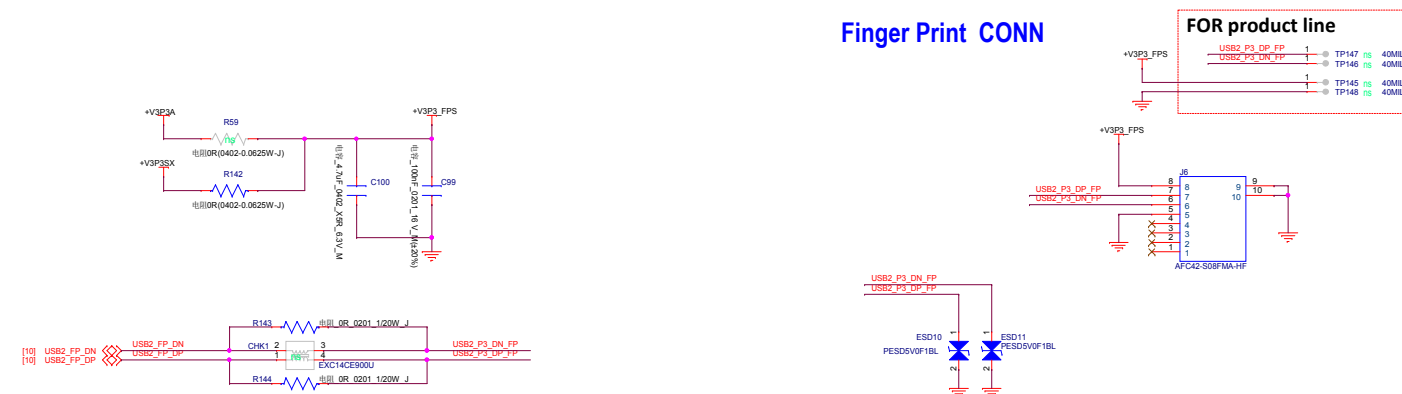
KB Backlight



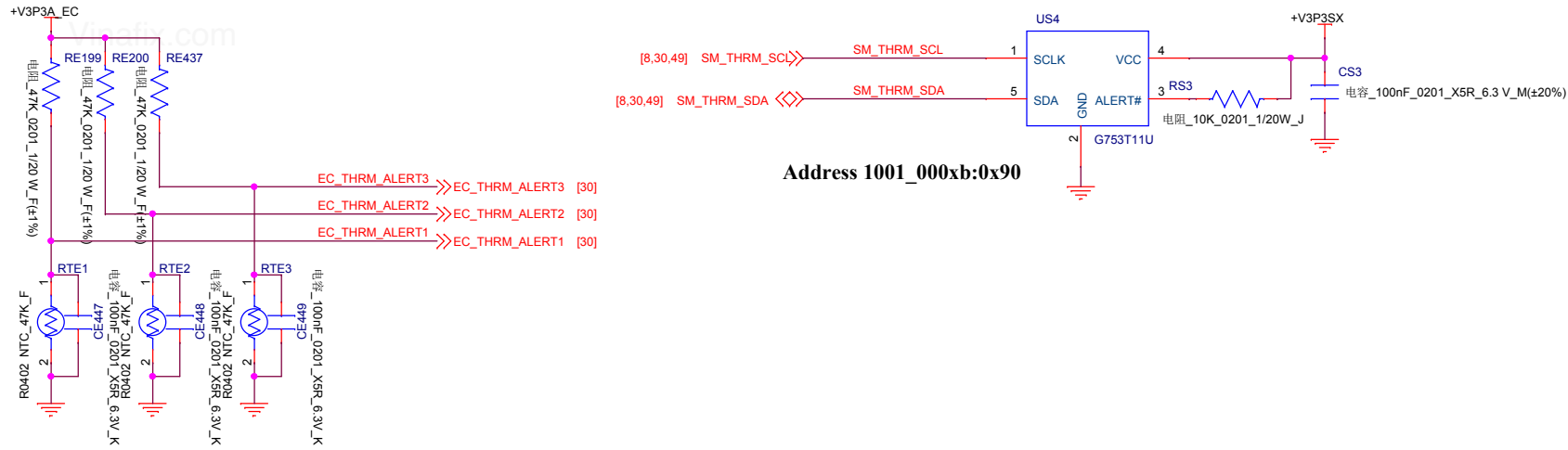
Finger Print



Finger Print CONN

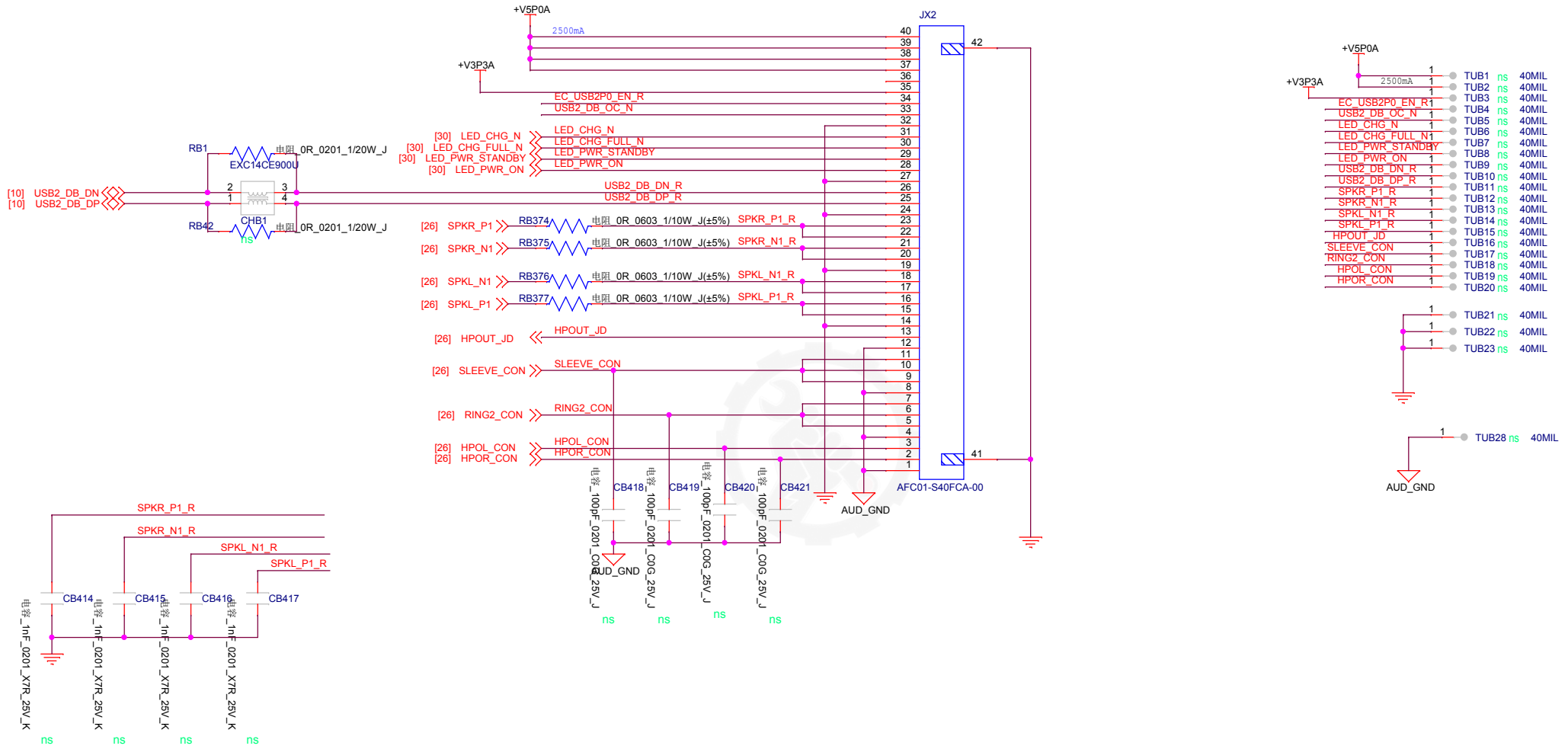


Thermal sensor

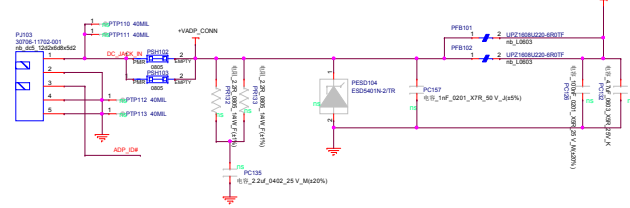


IO Board Conn

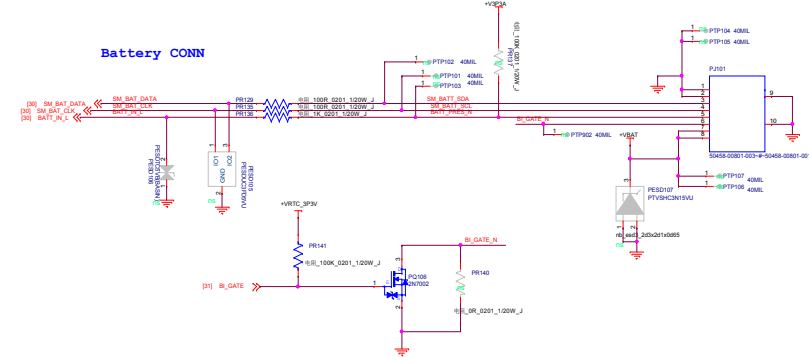
Vinafix.com



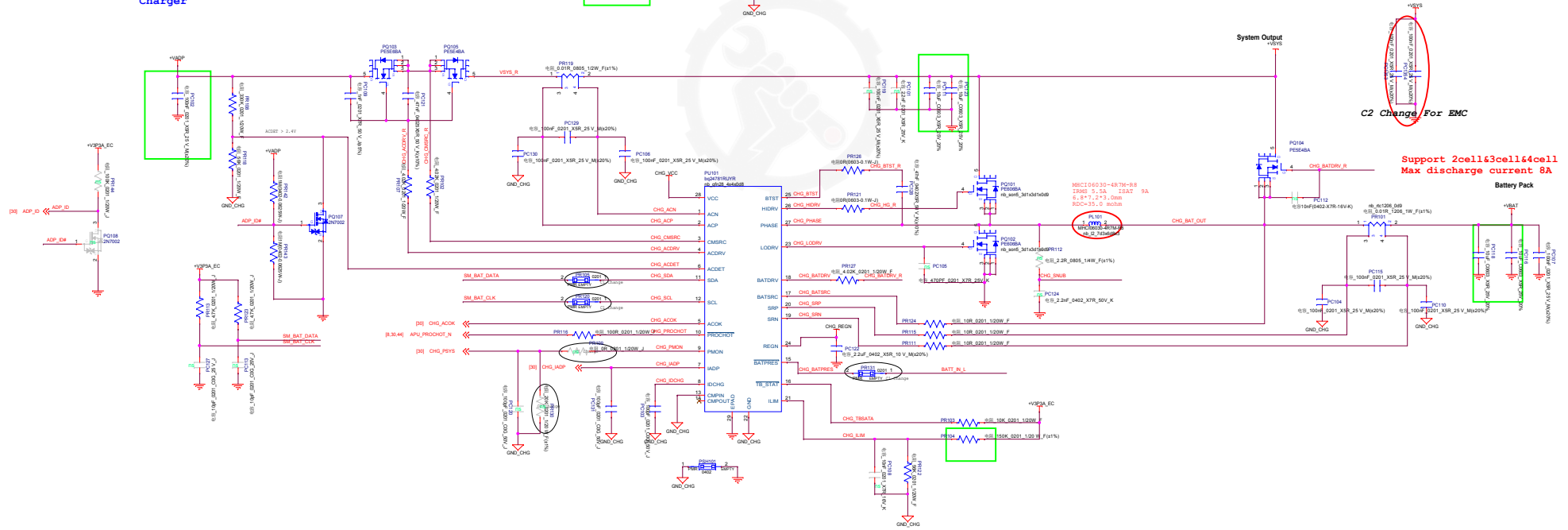
DC-IN



Battery CONN



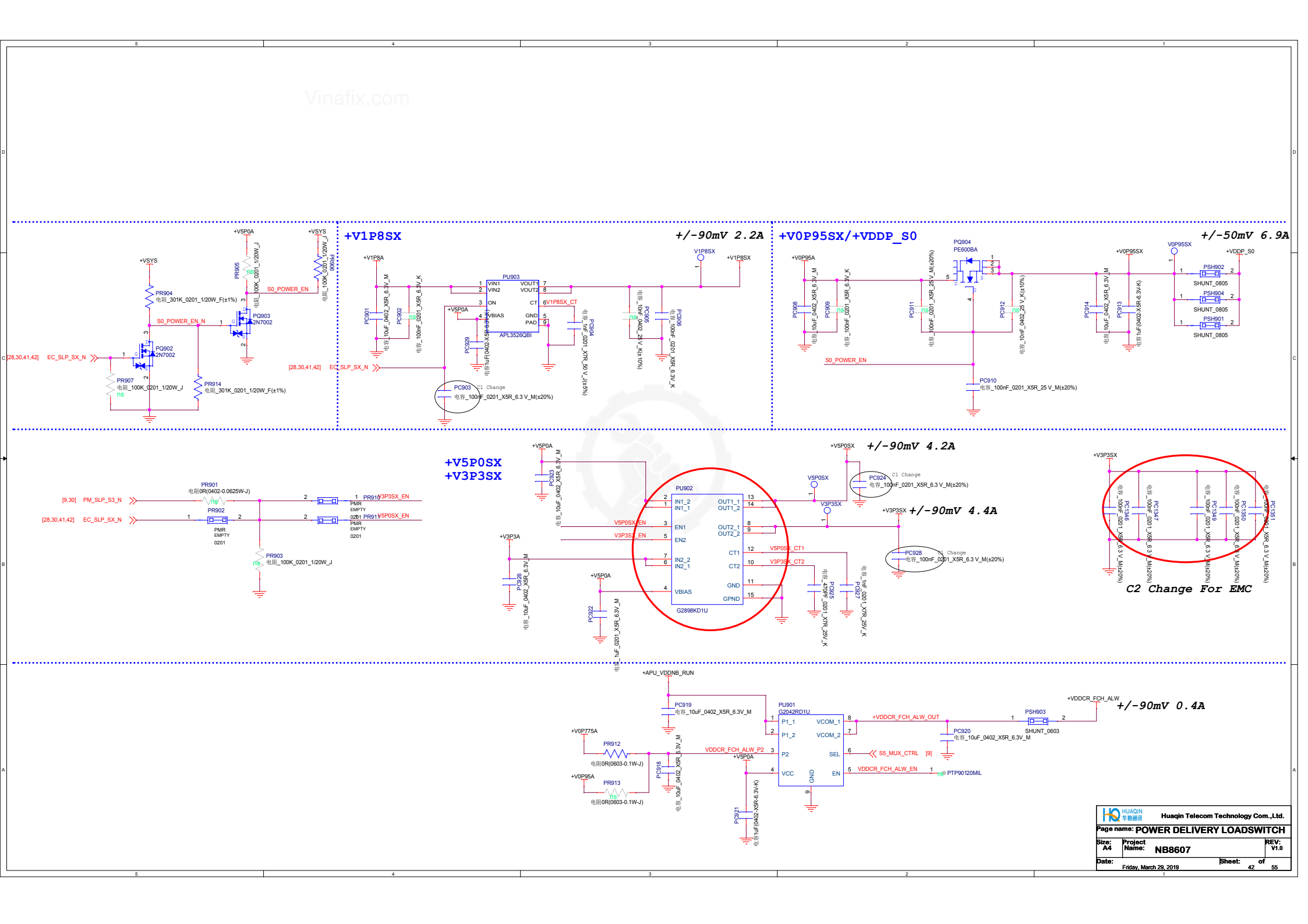
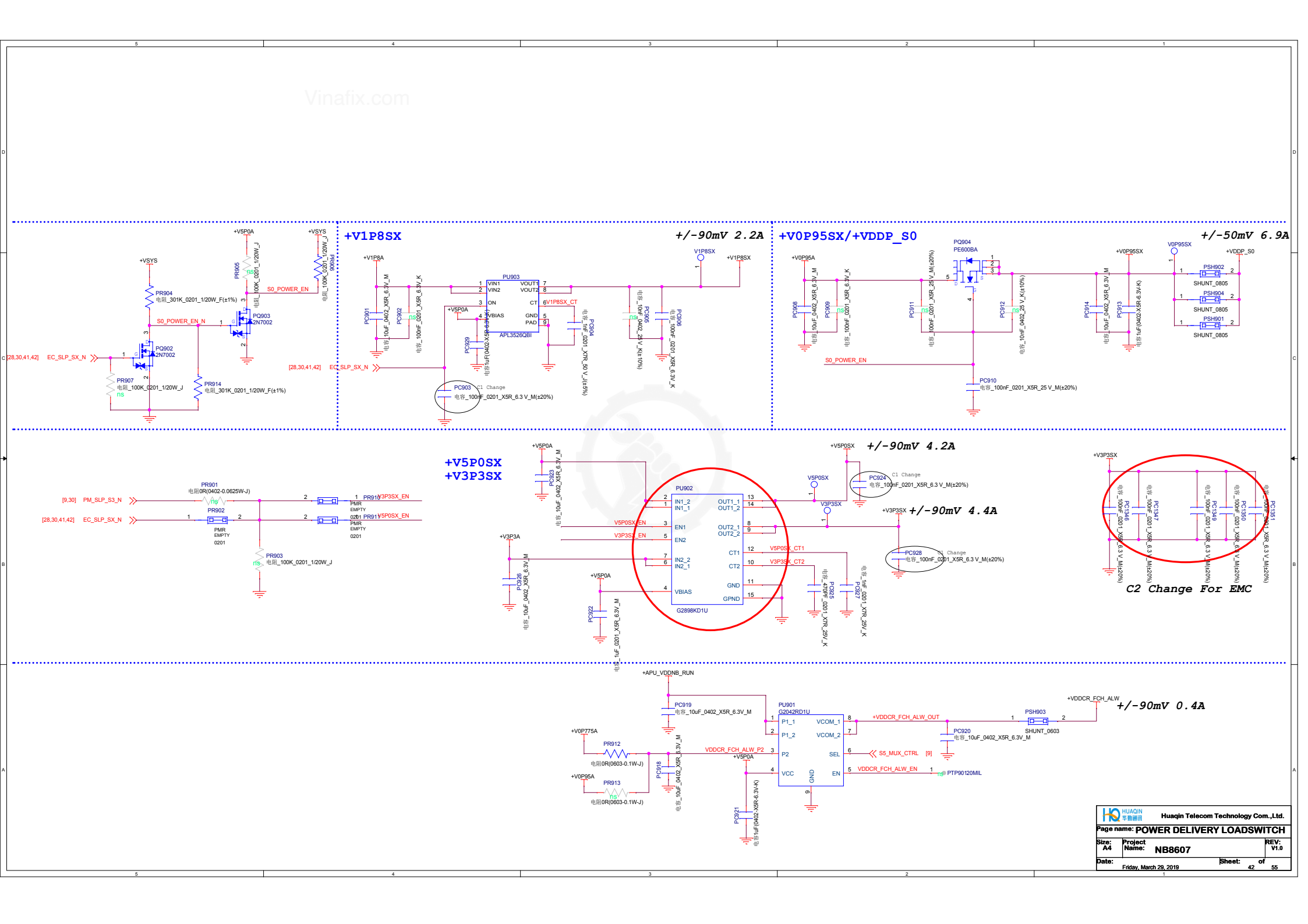
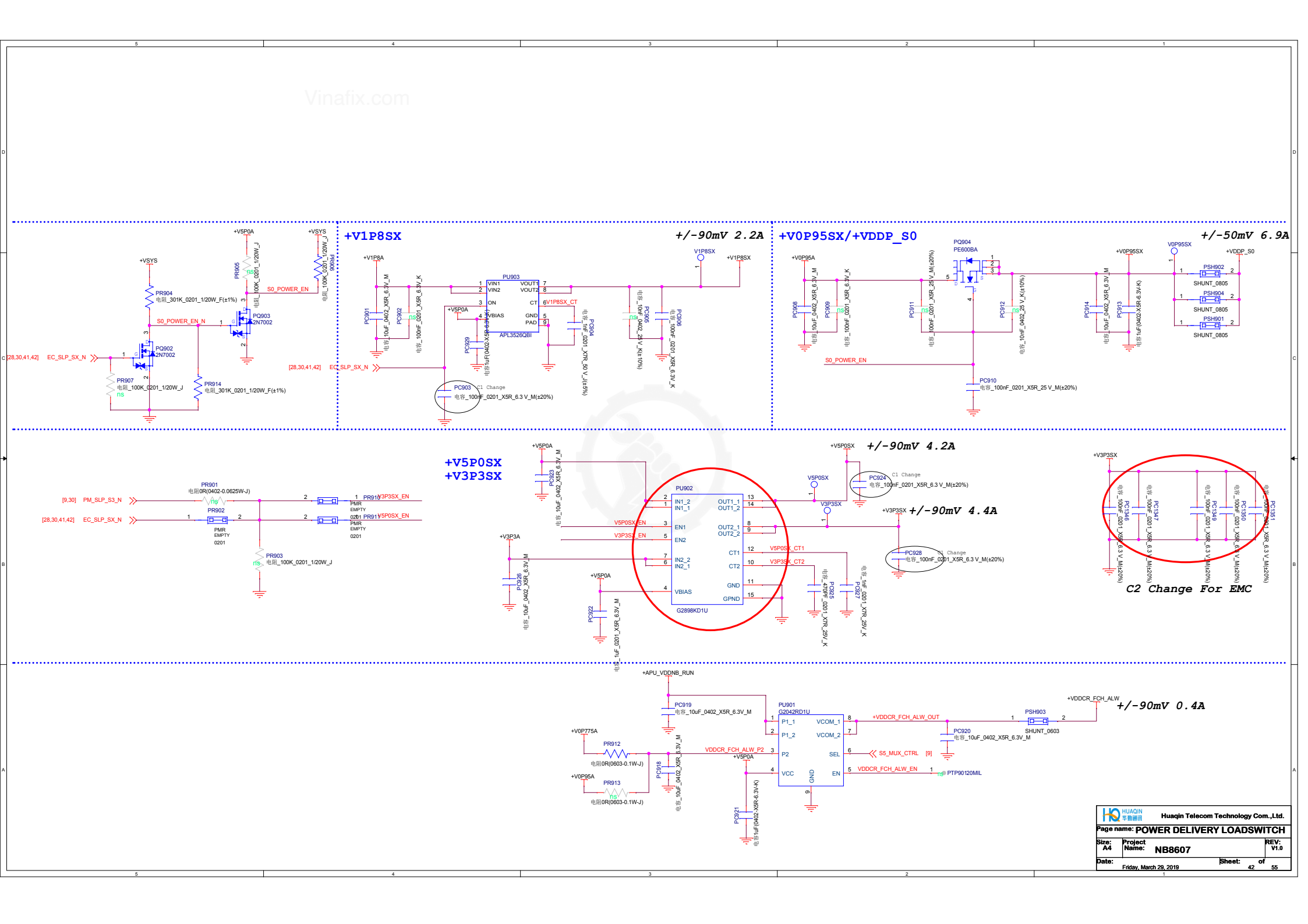
Charger



C2 Change For EMC


Support 2cell16cell4cell 48W
Max discharge current 8A

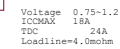
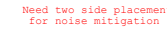
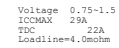
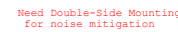
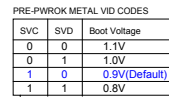
Battery Pack



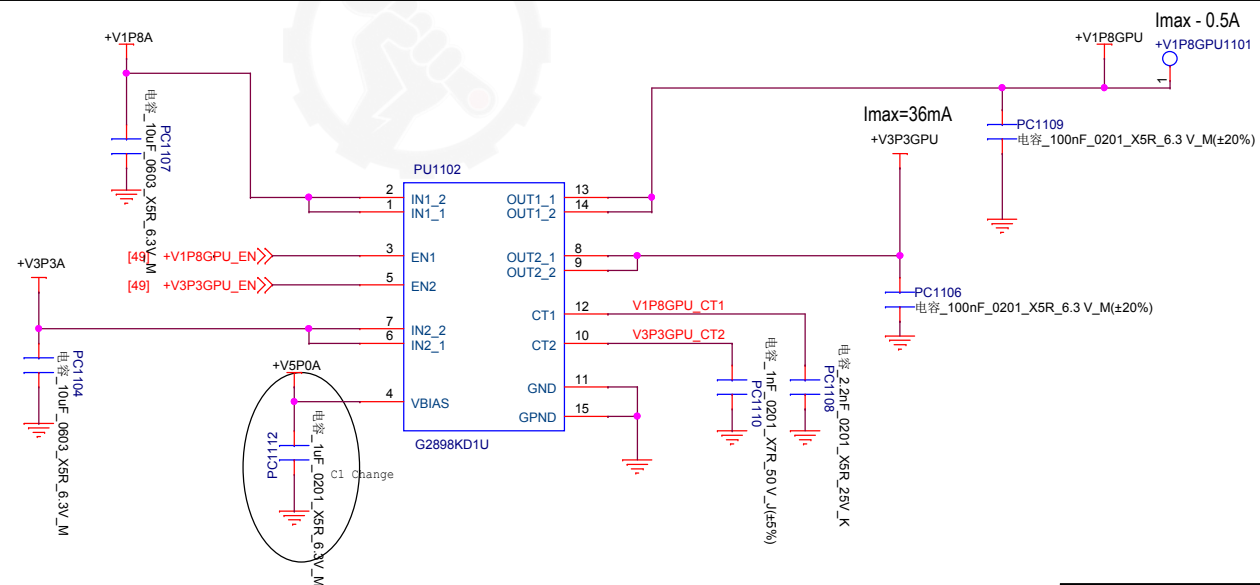
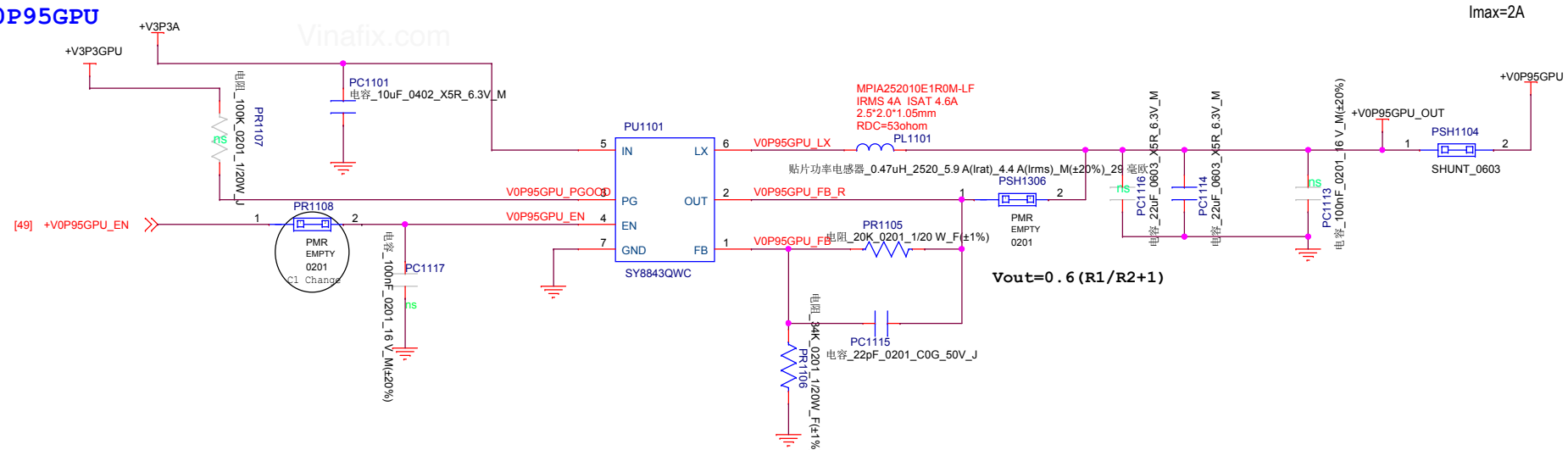
Vinafix.com



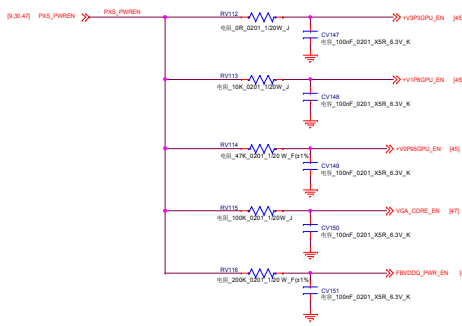
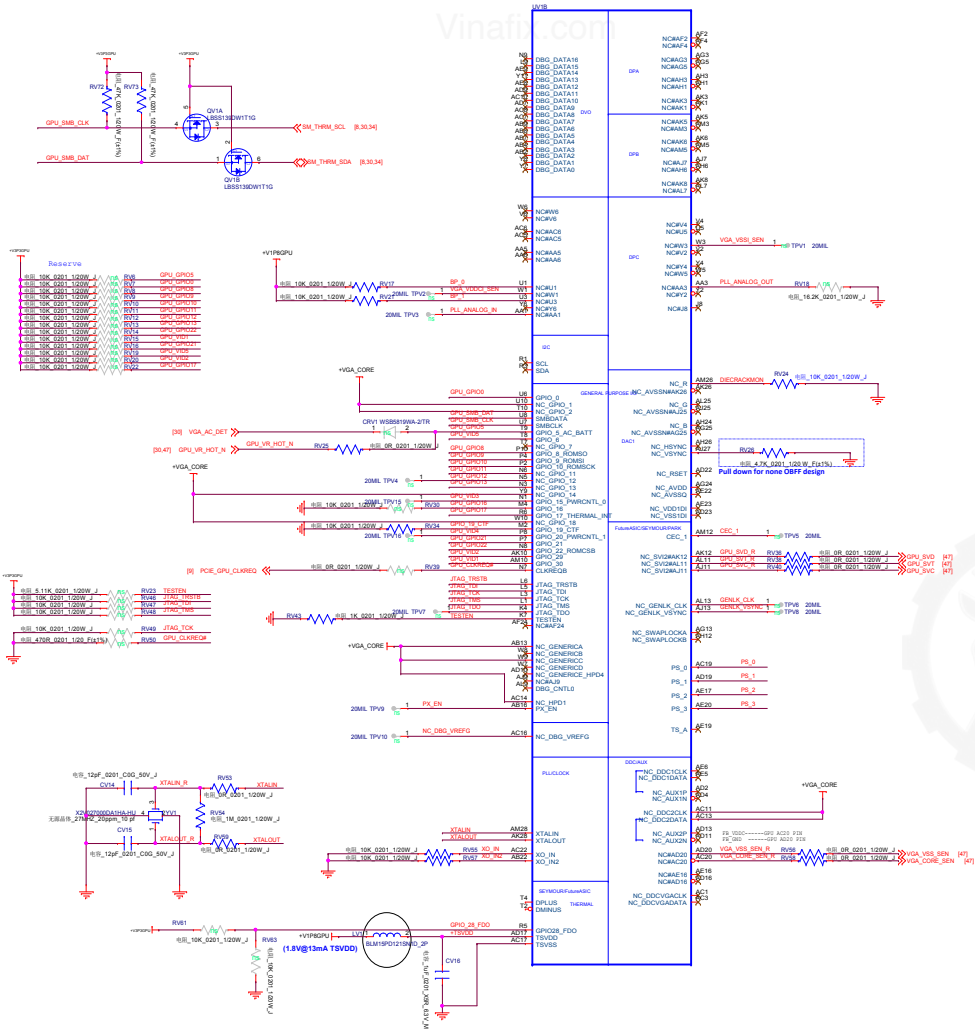
 HUAQIN 华勤通信		Huaqin Telecom Technology Com.,Ltd.	
Page name: POWER DELIVERY backlight			
Size: A4	Project Name: NB8607		REV: V1.0
Date:	Friday, March 29, 2019	Sheet: 43	of 55



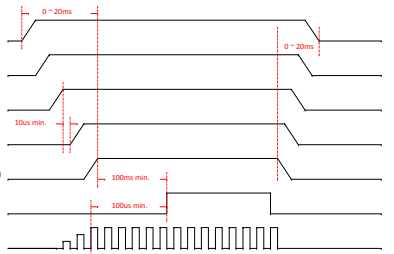
 Huaqin Telecom Technology Co., Ltd.	
Page name: CORE & NB	
Size: A4	Project Name: NB8607
Date: Friday, March 20, 2015	REV: V1.0



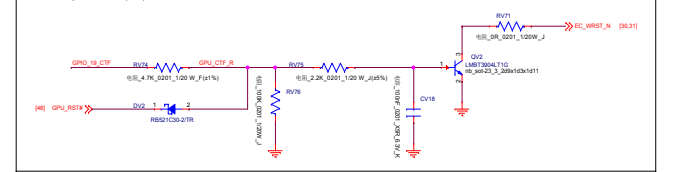




VDDR3(+V3P3GPU)
VDD_CT(+V1P8GPU)
PCIE_VDDC(+V0P95GPU)
VDDR1(+V1P35GPU)
VDDC/VDDCI(+VGA_CORE)
PERSTb(GPU_RST#)
REFCLK(CLK_PCIE_VGA)



Critical Temperature Fault (CTF)



SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

MLPS	BLT	ROM
PS_0[5:1]	1 1 0 0 1	RV27=8.45K RV32=2K
PS_1[5:1]	1 1 0 0 1	RV28=8.45K RV43=2K
PS_2[5:1]	1 1 0 0 1	RV44=4.75K
PS_3[5:1]	1 1 1 1 1	RV45=4.75K

with BOM structure control, RV43, RV45 change to different value to adjust VRAM config

with BOM structure control, when config REG3, RV28 change to 8.45K, RV33 change to 2K

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
9450	2000	001
4900	2000	010
1000	4900	011
4900	4900	100
3240	5020	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[5:1]	ROM_CONF00	Define the ROM type when STRAP_BIOS_ROM_EN = 1	001
PS_0[5:1]	ROM_CONF01	Define the primary memory export size when STRAP_BIOS_ROM_EN = 0	001<000000
PS_0[5]	NA	Reserved for internal use only. Must be 0 at reset.	1
PS_1[5]	NA	Reserved.	1
PS_1[4]	STRAP_BIF_GEN0_EN_A	1 = PCIe GEN0 is supported. 0 = PCIe GEN0 is not supported.	1 = GEN0 is supported
PS_1[3]	STRAP_BIF_GEN0_EN_B	1 = The CLAREDO power management capability is disabled. 0 = The CLAREDO power management capability is enabled.	0
PS_1[2]	NA	Reserved for internal use only. Must be 0 at reset.	0
PS_1[1]	STRAP_TX_GPIO_DRV_0	0 = The transmitter full swing is enabled. 1 = The transmitter full swing is disabled.	1 = Enable
PS_1[0]	STRAP_TX_GPIO_DRV_1	0 = Tx downswing disabled. 1 = Tx downswing enabled.	1 = Enable
PS_2[7]	NA	Reserved.	0
PS_2[6]	NA	Reserved.	0
PS_2[5]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0 = Disable
PS_2[4]	NA	Reserved.	1
PS_2[3]	NA	Reserved.	1
PS_2[2]	BOARD_CONFIG0	Board configuration related strap, such as for memory ID.	001 = 16MB 1G-10211100000 RV42=4.9K RV43=2K
PS_2[1]	BOARD_CONFIG1	Board configuration related strap, such as for memory ID.	001 = 16MB 1G-10211100000 RV42=4.9K RV43=2K
PS_2[0]	NA	Reserved.	1
PS_3[5]	NA	Reserved.	1



